An asymmetrical 175 kV, 210 ns Pichugin pulse generator

M Rivaletto, P Domens and P Pignolet

Laboratoire Génie Electrique, Université de Pau, 64000 Pau, France

Received 17 March 1998, in final form 21 May 1998, accepted for publication 19 June 1998

Abstract. The working of the Pichugin pulse generator (named after its Russian inventor) is accurately studied. The influences of inductance and capacitance on the output signal characteristics are studied. A theoretical expression for the output signal's rise time, versus the stage number and the component values, is established. A technical innovation, consisting of an asymmetrical structure which allows an important decrease in rise time and an increase in output peak voltage, is proposed. The realization of a 175 kV, 210 ns rise time, six-stage asymmetrical pulser is proposed and discussed. The improvement compared with the performances of the equivalent symmetrical pulser, for the same rise-time value, is about 50% more voltage.

Keywords: high voltage, rise time, pulse generator, high-voltage supply, coupled circuits, pulse transformer, pulsed power, spark gap trigger

1. Introduction

The Pichugin pulse generator [1] has the advantage of using one switch only to make several unresistive LC circuits oscillate. A three stage-generator of this type is represented in figure 1. Such a generator is interesting because it is made up of a stage including the switch, a stage connected to the load and a stage known as the middle. So, for generators with more stages, only the number of middle stages will be modified. The identical capacitors ($C_i = C$) are initially charged, with Sw_1 open, to a high voltage, V_{HV}. When $t = t_0$, we close Sw_1. The Pichugin pulser principle [2, 3] consists of the fast reversal of the even-numbered capacitors' polarity in relation to the much slower reversal of the odd-numbered capacitors' one. This device is worth using only when the coupling coefficient k of the 1:1 pulse transformers is very high ($k > 0.995$).

We previously established [3] that, for a one-stage pulser, the output crest voltage V_{Ocr} was reached when

$$t_{cr} = \pi (L_{TL} C_2)^{1/2} = \pi [2(1-k) L C_2]^{1/2} \qquad (1)$$

where L_{TL} is the transformer's total leakage inductance and L is the transformer's self-inductance. For a dc supply voltage V_{HV}, the output crest voltage will be

$$V_{Ocr} = V_{HV} \{1 + \cos\{\pi [2(1-k)]^{1/2}\}\} \qquad (2)$$

which is very close to $2V_{HV}$ if the generator is perfect.

We found another important result, namely that the current i_m producing the flux circulation in the ferrite core is equal to that which goes through the odd-numbered capacitor. Its amplitude and its frequency are much lower than those of the primary and secondary currents of the transformer. This current i_m can be expressed by

$$i_m(t) \approx i_{C_{2i+1}}(t) \approx V_{HV} \left(\frac{C_{2i+1}}{L}\right)^{1/2} \sin\left(\frac{t}{(LC_{2i+1})^{1/2}}\right). \qquad (3)$$

A Pichugin generator generates output pulses quicker than allowed by the magnetic core's high cut-off frequency and uses the ferrite very efficiently. If this generator is used up to the ferrite's saturation limit, this saturation stage experimentally appears when

$$t_{SAT} \approx \frac{\pi}{4} (LC_{2i+1})^{1/2}. \qquad (4)$$

In relation (4), we chose a $\pi/4$ coefficient rather than the theoretical one, $\pi/2$, because, by experiment, the saturation due to the magnetizing curve shape is revealed far before reaching its maximum theoretical value. Dividing this time by two means that the saturation appears at about 70% of this maximum theoretical value, which is confirmed by our experiments.

The main interest of the Pichugin generator lies in the fact that one can, theoretically, easily increase its voltage gain by increasing its number of stage n, the 'ideal' voltage gain being $2n$. By experiment, we got the expected increase in voltage gain but the output voltage's rise time increased too [3].

This increase in the output voltage's rise time is embarrassing for two reasons:

(i) because one looks for a rise time as short as possible in most applications; and

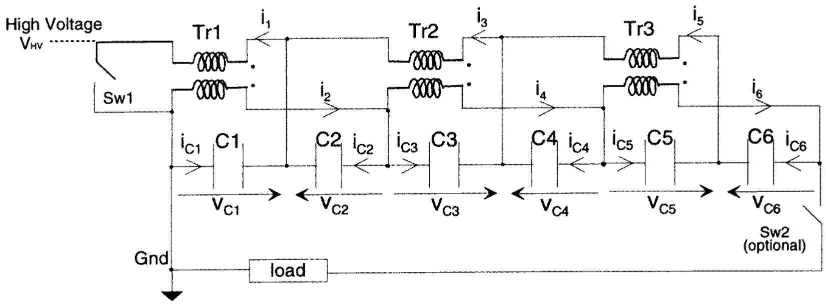

Figure 1. A three-stage Pichugin generator.

(ii) because, the ferrite's saturation time being independent of the number of stages, the amplification may be limited when the output's time to crest value, increasing in relation to n, will be close to t_{SAT}.

As shown in [3], the saturation is characterized by a faster and faster decrease in output voltage. In this example ($V_{HV} = 21$ kV, $C = 560$ pF, $L = 360$ μH, $k = 0.9965$ and $n = 4$), one more stage would be worthless insofar as the amplification is concerned. Therefore, it is necessary to reduce the output's time to crest value, while keeping t_{SAT} unchanged, in order to improve the generator's performance. To reduce this time, which is generally linked to the LC product, we will have to work on these parameters.

2. The *L* and *C* values' influences on the generator features

2.1. The influence of the transformer's self-inductance

The L value can be reduced by decreasing the number of turns, by diminishing the ferrite's volume or by using gaps or splitting the core. If the number of turns n_t is reduced, the coupling coefficient is perceptibly reduced too and we lose more in gain than we get in rise time [3, 4]. Thus, the diminution of n_t from 7 to 3 makes k go down from 0.9965 to 0.987 and the theoretical amplification for a three-stage generator decrease from 5.18 to 4.15. In [4] and for $n_t =$ constant, an important decrease in the performance of a three-stage pulser can be shown to occur when the k value is lower than 0.99: a decrease in gain and an increase in rise time are observed. So, a lower value of n_t will compensate for an increase in the rise time but not at all for a decrease in gain due to the decrease in k.

If the ferrite's volume is reduced then the dynamic of the applied V_{HV} voltage is reduced due to there being a lower saturation level. So, we can improve the rise time value to the detriment of the output voltage's maximum value, but the gain value is not greatly modified.

If one uses gaps or splits the core, while keeping the initial number of turns and volume unchanged, the coupling coefficient can be adjusted exactly to the desired value, versus the gap width (while keeping k greater than 0.995). The gap's presence allows a greater dynamic of the applied voltage V_{HV} and an increase in the output voltage's maximum value but to the detriment of a slight decrease in gain. The last method will be used to improve the pulser's performance.

2.2. The capacitor's influence

The relations (1) and (3) show that, if $C = C_{2i} = C_{2i+1}$ (the symmetrical case) decrease in C induces decreases in the rise time and in the magnetizing current. This allows a greater voltage dynamic of the pulser and an increase in the output voltage's maximum value. Nevertheless, that reduces the energy storage possibilities.

The t_{SAT} value decreases too but in proportion to t_{cr}, so this is not penalizing for the generator features. Consequently, we will use a reduction in capacitance when we wish to improve the rise time and the output voltage performance of the pulser. However, in a few cases, the transformer's stray capacitances will reduce these performances. Clearly, their influences will be more important when low-value discrete capacitors will be used (<2 nF). The stray capacitance's influence will be studied in the following section.

3. The asymmetrical principle

A reduction in the capacitance leads to decreases in the rise time (equation (1)) and in the gain, as shown in figure 2 ($V_{HV} = 5$ kV, $L = 1200$ μH and $k = 0.9982$ in our experiment). The study of the capacitors' waveshapes in relation to the C values and the number of stages reveals that the decrease in gain proceeds from the distortion of the odd-numbered capacitor waveshapes as shown in figure 3. When we use low-value capacitors (560 pF), the first observed distortion (like a droop) of all the odd-numbered capacitors' waveshapes appears at $t \approx t_{cr}$, so the distortions of all the $v_{C_{2i+1}}$ voltages are added and they induced a decrease in gain. Under the same conditions, the even-numbered capacitors' voltage shapes hardly change; their frequencies only decrease weakly.

For a one-stage generator, it is easy to represent the main stray capacitances of the transformer and to study their respective influences. Because we have shown [3, 4] that the number of stages had no great influence on the odd-numbered capacitor's waveshapes, for pulsers with more stages the results will be similar even though it is more difficult to study them.

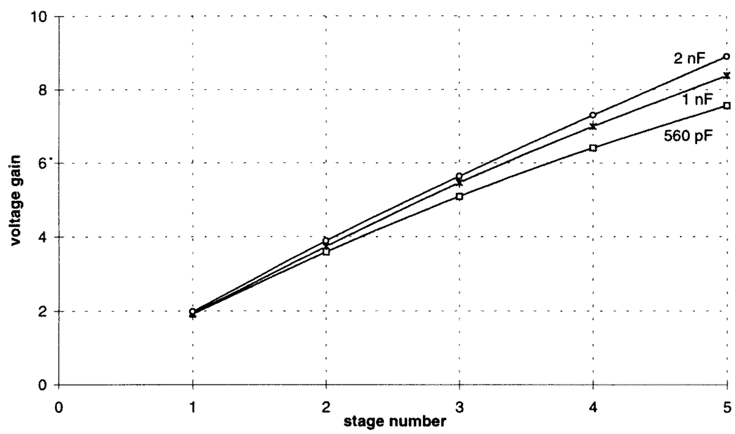

Figure 2. The voltage gain versus the number of stages for three capacitor types for a symmetrical generator.

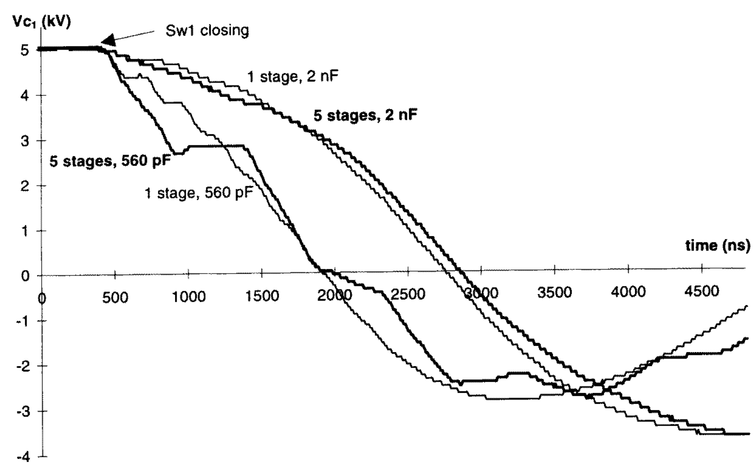

Figure 3. The voltage V_{C_1} for a one-stage and a five-stage generator (C_1 = 560 pF and C_1 = 2 nF).

We will study only the influences of the input stray capacitance (C_{Si}), the output stray capacitance (C_{So}) and the coupling stray capacitance (C_{Sio}), which appear in figure 4. The C_{Si} and C_{So} values can be estimated to be about 100 pF. The C_{Sio} value depends on the number of turns of winding, the distance between cable windings and the type of winding, so it can vary from 50 to 100 pF or more. Since the C_{Sio} stray capacitance is in parallel with C_2, it influences only and weakly the frequency of the voltage v_{C2}.

Concerning C_{Si} and C_{So}, their influences are not easy to estimate, so, using MicroSim Design Center 6.2 [5], we simulated this phenomenon as is represented in figure 5. We used a five-stage device ($V_{HV} = 5$ kV, $C = 560$ pF, $L = 1200$ μH and $k = 0.9982$) and simulated the $v_{C1}(t)$ voltage without any stray capacitance and with a 100 pF output stray capacitance on each transformer.

When comparing figures 3 and 5, it is evident that the decrease in gain is tightly linked to the growing influence of the output stray capacitances while the generator's own capacitances are reduced. Consequently, the idea of producing an asymmetrical device by decreasing only the even-numbered capacitances seems interesting.

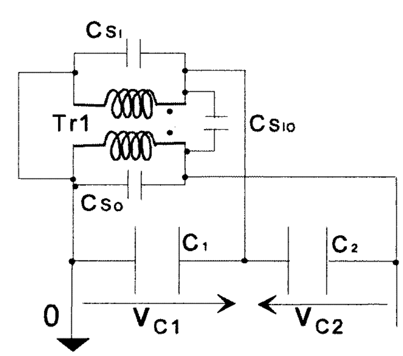

Figure 4. The one-stage-generator equivalent scheme, with stray capacitances.

Our experimental results for $C_{2i+1} = 2$ nF and $C_{2i} = 560$ pF compared with those in the symmetrical device for $C_i = 2$ nF are quite exciting (figure 6): we obtained a significant improvement in the rise time value without any lack of gain but on the contrary a slight increase (4%). The quantitative experimental results obtained for two symmetrical devices (the one with 2 nF capacitors and

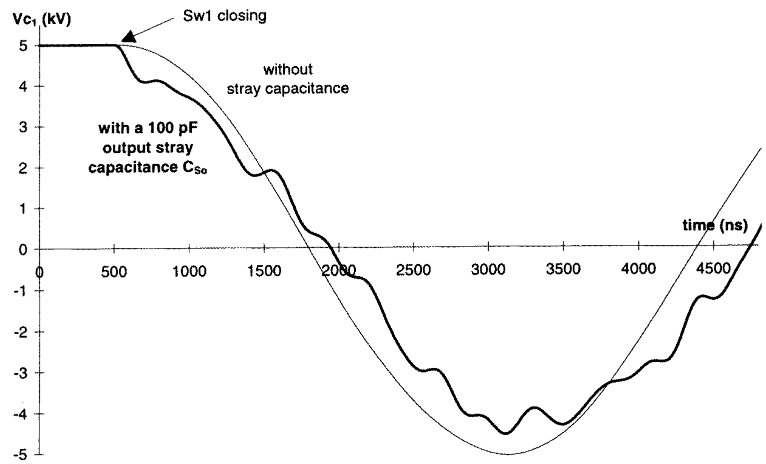

Figure 5. The simulated voltage V_{C_1} (C_1 = 560 pF) with an output stray capacitance (100 pF) and without an output stray capacitance C_{So} for a five-stage generator.

Table 1. The voltage gain and time to crest for two symmetrical generators (2000 and 560 pF) and for an asymmetrical one (2000 plus 560 pF).

C_{2i+1} (pF)	C_{2i} (pF)	Voltage gain	t_{cr} (ns)
2000	2000	5.1	452
560	560	4.6	233
2000	560	5.2	246

the other with 560 pF capacitors) and for the asymmetrical one above ($C_{2i+1} = 2$ nF and $C_{2i} = 560$ pF) are given in table 1.

If we write $C_{2i} = C_{2i+1}/m$, we notice that the rise time value of the asymmetrical device is almost equal to that of the symmetrical one (based on C_{2i+1}), divided by $\sqrt{m}$ (this is confirmed later by equation (11)). In order to keep on improving the performance of this type of generator, we will focus our study upon this time to crest which has some influence on the amplification limits.

4. The time to crest and rise time of the output voltage

The results in [3] permit an analysis of the variations in time to crest (t_{cr}) versus the number of generator stages ($V_{HV} = 4$ kV, $C = 2$ nF, $L = 1200$ μH, $k = 0.9982$ and $n = 1$–5). We did the same with $C = 560$ pF and 1 nF. The results for the time to crest in these 15 configurations (and those got after simulation using MicroSim software) are reported in figure 7.

The variations $t_{cr} = f(n)$ are linear and can be roughly represented as follows (times are in nanoseconds):

$$t_{cr}(n) = 80.5n + 62.5 \qquad \text{for } C = 560 \text{ pF} \qquad (5)$$

$$t_{cr}(n) = 114n + 76 \qquad \text{for } C = 1 \text{ nF} \qquad (6)$$

$$t_{cr}(n) = 158n + 114 \qquad \text{for } C = 2 \text{ nF}. \qquad (7)$$

However, we notice a slight difference between the experimental and simulated t_{cr} values. More precisely, the experimental value is lower than the simulated one; consequently this cannot be imputed to any stray capacitances. We infer that this difference arises rather from the uncertainty in the measurement of k [4]; an absolute error of 10^{-4} is enough to cause it.

Now, it would be interesting to correlate the t_{cr} values to those of the generator's components. For a one-stage generator, we showed (1) that

$$t_{cr}(1) = \pi[2(1-k)LC_2]^{1/2}. \qquad (8)$$

Since the t_{cr} variations according to n are linear, we can write, to a first approximation:

$$t_{cr}(n) = t_{cr}(1) + (n-1)t_s. \qquad (9)$$

If we write the relations (5)–(7) and take those obtained by simulation into account, in the form of (9), we realize that $t_s \approx 2t_{cr}(1)/\pi$, that is to say

$$t_{cr}(n) = \pi[2(1-k)LC_{2i}]^{1/2} + 2(n-1)[2(1-k)LC_{2i}]^{1/2} \qquad (10)$$

or also

$$t_{cr}(n) = [2(n-1) + \pi][2(1-k)LC_{2i}]^{1/2}. \qquad (11)$$

These theoretical $t_{cr}(n)$ values (obtained by using (11)) are also presented in figure 7.

These previous results and remarks relate to symmetrical devices. They remain valid for asymmetrical generators.

We remark that the rise time, t_r, can be classically defined as 10–90% of V_{Ocr}, but, because of the type of the output signal's shape, we have shown [4] that t_r could be estimated to be about 66% of t_{cr} for the generators with more than three stages.

5. The ferrite's saturation

The ferrite's saturation is one of the main factors limiting the voltage of the Pichugin generator by restricting the number of stages that can be used. This limitation condition can be written

$$t_{cr}(n) \leq t_{SAT} \qquad (12)$$

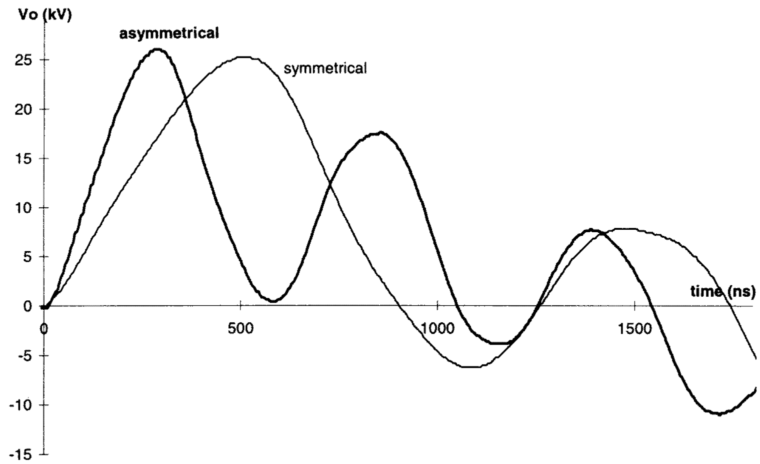

Figure 6. The influence of an asymmetrical structure on the measured output voltage of a three-stage generator.

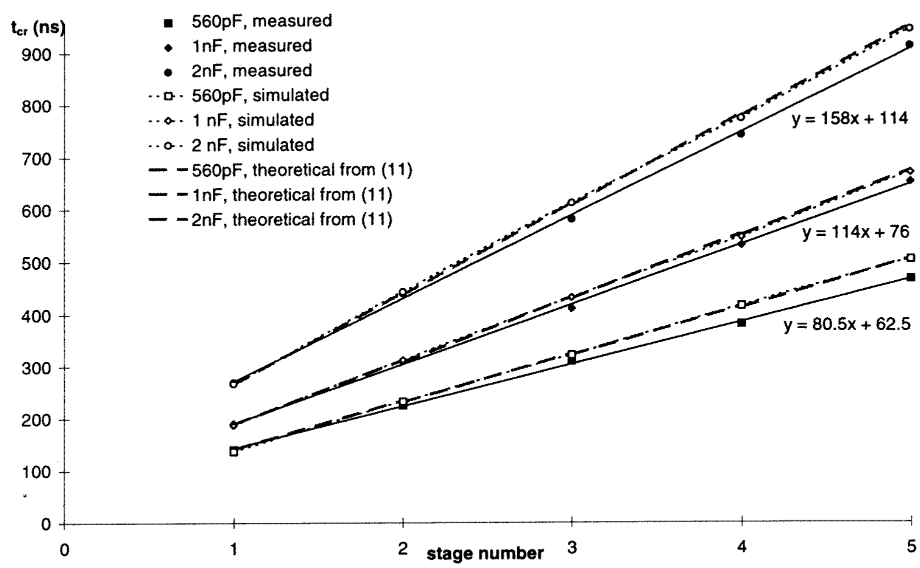

Figure 7. The time to crest versus the number of stages (measured, simulated and calculated from equation (11)).

which gives, in the case of asymmetrical generators and from the relations (4) and (11):

$$[2(n-1)+\pi][2(1-k)LC_{2i}]^{1/2} \leq \frac{\pi}{4}(LC_{2i+1})^{1/2} \quad (13)$$

from which

$$n \leq 1 + \frac{\pi}{2}\left(\frac{\sqrt{m}}{4[2(1-k)]^{1/2}} - 1\right) \quad (14)$$

where $m = C_{2i+1}/C_{2i}$. Thus, for $k \approx 0.9965$ and in a symmetrical case ($m = 1$), the relation (14) gives $n \leq 4.12$.

The flux in the ferrite core is created by the current going through the odd-numbered capacitors. Consequently, both devices, the symmetrical one and the asymmetrical one with odd-numbered capacitors of equal values and with identical transformers, will be saturated, for the same input voltage, at the same moment (relation (3)).

In the case of an asymmetrical generator, for which for example $C_{2i+1} = mC_{2i} = 4C_{2i}$, the inequality (14) leads to $n \leq 8.82$ and it is interesting to compare it with the value 4.12 obtained before in the symmetrical case.

Theoretically, we can therefore establish that, at a constant time to crest close to t_{SAT}, the asymmetrical choice allows one, by increasing the number of stages, to multiply the voltage gain by $\sqrt{m}$. By experiment, in the example above, we reached a multiplication factor of 1.8 instead of 2.0.

This conclusion is valid only if the working conditions of the generator are close to magnetic saturation, which is the case when a generator works at its maximum performance (maximum output voltage). If the cores are not saturated, increasing the number of stages is not a problem.

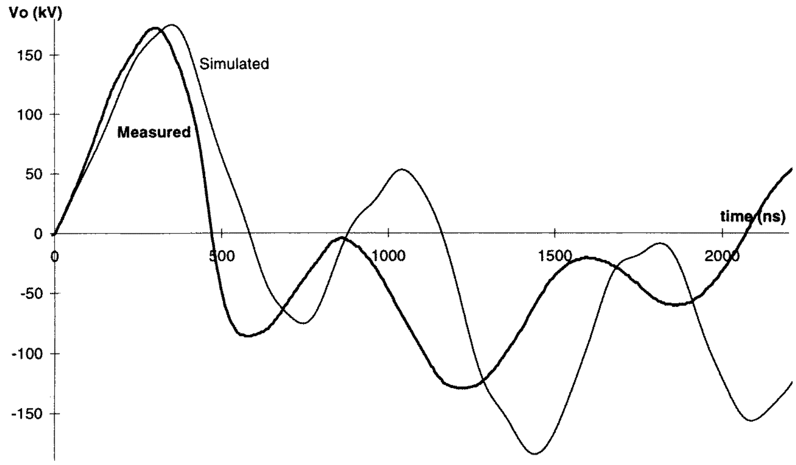

Figure 8. Measured and simulated output waveshapes produced by the six-stage asymmetrical generator (V_{HV} = 23 kV, C_{2i+1} = 560 pF, C_{2i} = 140 pF, L = 360 μH and k = 0.9965).

6. The realization

6.1. The component's values

We use a 23 kV (maximum value) dc power supply to produce, at least, a 180 kV pulse with a rise time close to 200 ns. We have shown [3, 4], that the voltage gain increased with the number of stages and with the capacitance (figure 2) but the rise time increased too (figure 7). So, our conclusion was that, in order to produce the highest voltage in the shortest rise time, it is necessary to minimize the number of stages and maximize the dc V_{HV}.

In the same study (figure 2), we showed that the first value of the number of stages for which the voltage gain is greater than 8, was five, if we used 2 nF capacitors, or six, if we used 560 pF capacitors. We chose the second value, for the following reasons.

For a six-stage generator, the rise time can be deduced from the relation (11) by

$$t_m(6) \approx \frac{2t_{cr}(6)}{3} = \frac{2}{3}(10+\pi)[2(1-k)LC_{2i}]^{1/2}. \quad (15)$$

If we respect the conditions established in section 2.1, namely a sufficient number of turns, a significant ferrite volume and a gap to increase the pulser's voltage dynamic, the transformer built in the laboratory has the features $L \approx 360$ μH and $k \approx 0.9965$. The ferrites and LCC B1 material ferrite cores [6] which are split to adjust the saturation limit. Their total air gaps are about 300 μm and the number of turns is seven. Under these conditions, the magnetization current's maximum value is about 30 A.

By using the relation (15), it is possible to calculate the maximum capacitance consistent with providing a rise time lower than 200 ns. The relation gives 210 pF. If we choose a symmetrical structure, built with 210 pF capacitors, figure 2 shows that the voltage gain will be surely lower than 8 for a six-stage generator, which is due to the stray capacitance's influence. So we decided to use an asymmetrical generator and 210 pF will be the even-numbered capacitors' value.

Owing to the influence of the coupling stray capacitances (they are in parallel with the C_{2i} capacitors and are evaluated to be 50–100 pF per transformer) when we use low-value even-numbered capacitors, the 210 pF value will be the sum of the coupling stray capacitances of the transformer and the discrete even-numbered capacitors. So, the discrete component's value will be chosen between 160 pF $(210-50)$ and 110 pF $(210-100)$. The commercial components available are 140 pF.

The odd-numbered capacitors' value must be calculated by considering the saturation limit, the stray capacitance's influence and the initially stored energy. In a previous realization [3], we showed that, by using the same transformers, the 560 pF odd-numbered capacitors saturated the ferrite at $V_{HV} \approx 25$ kV. Knowing that this dc voltage is close to the V_{HV} value required for reaching 180 kV, we chose this type of odd-numbered capacitors.

6.2. The experimental results and comments

We built a six-stage pulser with $C_{2i+1} = 560$ pF, $C_{2i} = 140$ pF and $L = 360$ μH ($k \approx 0.9965$) triggered by a trigatron switch. The dc V_{HV} value is 23 kV. The 560 pF capacitors are TDK ceramic ($SrTiO_3$) knob-type capacitors [7] whereas the 140 pF ones are of the same type but from Thomson LCC [8]. The generator output pulse's waveshape is shown in figure 8.

We measured a voltage peak value of about 175 kV with a 210 ns rise time (the time to crest is about 300 ns). The repetition rate is close to 10 Hz and must be increased by modifying the switch configuration.

On the pulse shape, at about time 450 ns, we could notice a faster decrease of the pulse, due to the core's partial saturation. We noticed the same phenomenon, at about the same dc V_{HV} and time values, in a previous realization [3]. In this paper, the pulser was symmetrical, had four stages and its voltage peak value was about 117 kV with a 220 ns rise time. We concluded that adding a stage will not lead to a noticeable increase in voltage gain. So, we can remark how much the asymmetrical structure can improve the generator's performance. By comparing the two realizations, we can conserve approximately the same rise time value (210 versus 220 ns), but we can increase the output peak's value by about 50% (from 117 to 175 kV).

Two phenomena can modify the expected theoretical features of the output signal, namely the saturation of the ferrite cores and the transformer's stray capacitances. By using MicroSim software, it is easy to simulate the stray capacitance's presence. If we simulate the pulser's behaviour, with $C_{Si} = C_{So} = 100$ pF at the input and output ends of each transformer and with $C_{Sio} = 50$ pF, the simulated output signal has a peak value equal to the measured one but a rise time value of 240 ns. This signal is shown in figure 8. The difference between the measured and simulated rise times can be explained by considering the ferrite core's saturation. This phenomenon decreases the inductance and the voltages v_{C2i} oscillate faster.

7. Conclusions

In this paper, we described thoroughly an improvement to the Pichugin pulse generator. We established a relation which gives the output voltage's rise time versus the number of stages and the component's values. This relation allowed us to propose as an improvement an asymmetrical structure. An asymmetrical generator has a lower output rise time than does the symmetrical equivalent one, so this structure allows an increase in the number of stages and therefore the output peak voltage, when the ferrite cores operate as close as possible to their saturation limit.

When a very short rise time is required, this method is an obvious improvement, but the use of low-value capacitors increases the stray capacitance's influence. This phenomenon reduces the voltage gain but does not modify the expected rise time.

References

[1] Pichugin Yu P, Rezyukov I V and Romanenko I N 1981 Pulse voltage generator, USSR patent 812725 (1985 translated by Foreign Technology Division, FTD-ID(RS)T-0541-85)

[2] Engel T G, Kristiansen M and Bridges J 1993 A compact 100 kV nanosecond pulser *Proc. 9th IEEE Int. Pulsed Power Conf.* pp 107–9

[3] Rivaletto M, Domens P and Pignolet P 1998 Inner wave shape characterization and realization of a Pichugin pulse generator *Meas. Sci. Technol.* **9** 824–31

[4] Rivaletto M 1997 Conception de générateurs de fortes puissances pulsées: mise en forme et caractérisation de l'impulsion haute tension *Thèse* Université de Pau

[5] MicroSim Design Center V6.2, MicroSim Corporation, USA

[6] 1993 *Soft Ferrites* LCC Thomson CSF, France (data books of components)

[7] 1988 *High Voltage Ceramic Capacitors, BBE-003B* TDK Corporation, Japan (data books of components)

[8] 1993 *Condensateurs céramiques haute tension et de puissance* LCC Thomson CSF, France (data books of components)