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A high-voltage, high-frequency linear amplifier/driver for capacitive loads

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Abstract. A linear amplifier capable of providing a single-ended output in excess of 3 kV across a predominantly capacitive load requiring charge/discharge currents of order 10 mA is described. High-voltage capability, low-power consumption and excellent linearity and harmonic distortion performance are all obtained from a simple circuit, employing negative voltage feedback around a high-voltage low-power MOSFET ladder. Results are presented which highlight the performance of the amplifier in its intended role as a triangular-wave voltage driver for an electro-optic crystal.

1. Introduction

Linear amplifiers capable of high-frequency operation in the kilovolt range find use in several areas of applied physics, for example as actuators in piezo-transducer systems and as drivers for electro-optic (EO) modulator crystals and liquid cells (Wilson and Hawkes 1987). The amplifier described here was intended for use in a linear FM-chirped CO_2 laser system incorporating an intracavity CdTe EO modulator (Park and Williams 1989, Henderson *et al* 1989). In order to achieve the desired FM chirp range, rate and accuracy, a triangular drive voltage across the crystal of up to 7 kV peak-to-peak amplitude at frequencies in the range 500 Hz to 7 kHz was required, with a maximum deviation from linearity of less than 0.1%. Power consumption was also at a premium with a nominal target of 60 W from a 48 V DC supply.

Triangular waveform fidelity represents a particularly challenging problem in this application as the predominantly capacitive load of crystal plus connecting leads (around 50 pF was anticipated) requires the amplifier to source and sink a constant current of several mA on alternate half-cycles and, in addition, a wide small-signal bandwidth (of order 1 MHz) is needed if the amplitude and phase relationships of the Fourier components are to be accurately reproduced. Although a number of kilovolt solid state amplifiers have been described in the literature, none appear to combine all of the features required, being either frequency-limited (Skurnik 1986, Krasnov and Fomin 1988), excessively nonlinear (Theophanous *et al* 1988) or otherwise unsuitable on grounds of output voltage or power consumption.

The following sections of this paper include a discussion of the design and the implementation of an amplifier capable of achieving the performance outlined above, the test procedures adopted and results obtained under simulated service conditions. Where appropriate, comparisons are made with contemporary designs, and additional potential applications are suggested.

2. Design considerations

In maintaining a time-varying voltage V across a capacitive load C_L an instantaneous current $I = C_L\,dV/dt$ must be sourced or sunk by the drive circuitry. This may be achieved with optimal power economy by means of a class-B push–pull topology which, although straightforward at low output voltages, becomes unwieldy in the kilovolt range owing to the need for DC isolation between the (low voltage) driver stage(s) and the (high voltage) output stage. Optical isolation may be used for this purpose but will introduce significant nonlinearity if used in open loop (Theophanous *et al* 1988) and may introduce instability if overall negative feedback is applied.

A class-A resistive pull-up amplifier need not suffer from these problems (unless several output stages are series connected), but is wasteful of power owing to the need for a comparatively low fixed charging resistance and consequent high quiescent current. It may readily be shown that when driving a capacitive load with a triangular voltage waveform, the power consumption of otherwise comparable class-B and class-A amplifiers differs by a factor of approximately ten, and also that the class-A arrangement requires a substantially higher DC supply voltage. A compromise between ease of interstage coupling and power consumption is afforded by adopting class-A topology with the charging resistor replaced by a constant-current source, as shown in figure 1. Here, the power consumption at the slew-rate limit $I_0 = C_L\,dV/dt$ is just twice that of a class-B ampli-

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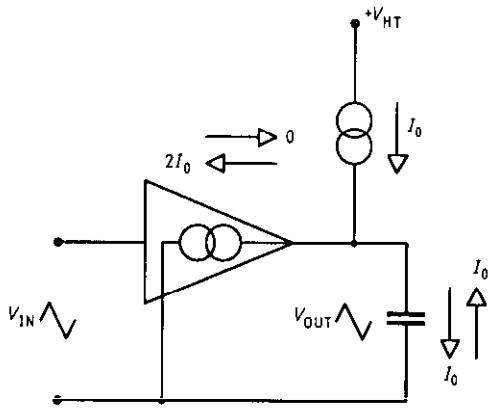

Figure 1. Class-A amplifier with constant current source providing triangular voltage drive to a capacitive load.

fier, as a constant current I_0 is drawn from the supply over a complete cycle. A similar approach has been adopted previously (Wenders 1989) for a somewhat different application.

In our particular case, the crystal capacitance C_x and connecting cable capacitance to ground C_c were around 30 pF and 20 pF respectively. Thus with two 3.5 kV amplifiers driven as an anti-phase bridge to provide a 7 kV excursion over 70 μs we have $dV/dt = 100\ V\ \mu s^{-1}$ and $I_0 = (C_x + C_c/2)\, dV/dt = 4$ mA, resulting in a power consumption of 14 W per amplifier, or 28 W total. This figure is within the power budget of 60 W even allowing for a modest 50% DC/DC conversion efficiency. The above figure indicates a need to dissipate powers in the 'power transistor' bracket, yet currents of only 10 mA or so need be controlled. As parasitic device capacitances scale roughly linearly with maximum current rating, the use of power transistors in this application is not attractive from the point of view of AC performance, and one is therefore led to consider the alternative strategy of power sharing in smaller devices having similarly high breakdown voltages. Preliminary investigations revealed that the SIPMOS 1 W *n*-channel MOSFETs BSS125 (enhancement) and BSS135 (depletion) could be reliably operated in series ladder connection, with their gates biased from a potential divider chain, at voltages approaching the quoted breakdown values of 600 V (Siemens 1987). Furthermore, it appeared that parasitic capacitances were sufficiently low to permit the use of relatively high-value biasing resistors, enabling power economies to be made without seriously compromising AC response. After several revisions, the final amplifier circuit shown in figure 2 was obtained and is described below.

3. Amplifier circuit

3.1. MOSFET ladder

Twelve MOSFETs, Q13 to Q24, and associated biasing resistors form the constant-current source. Q13 is a

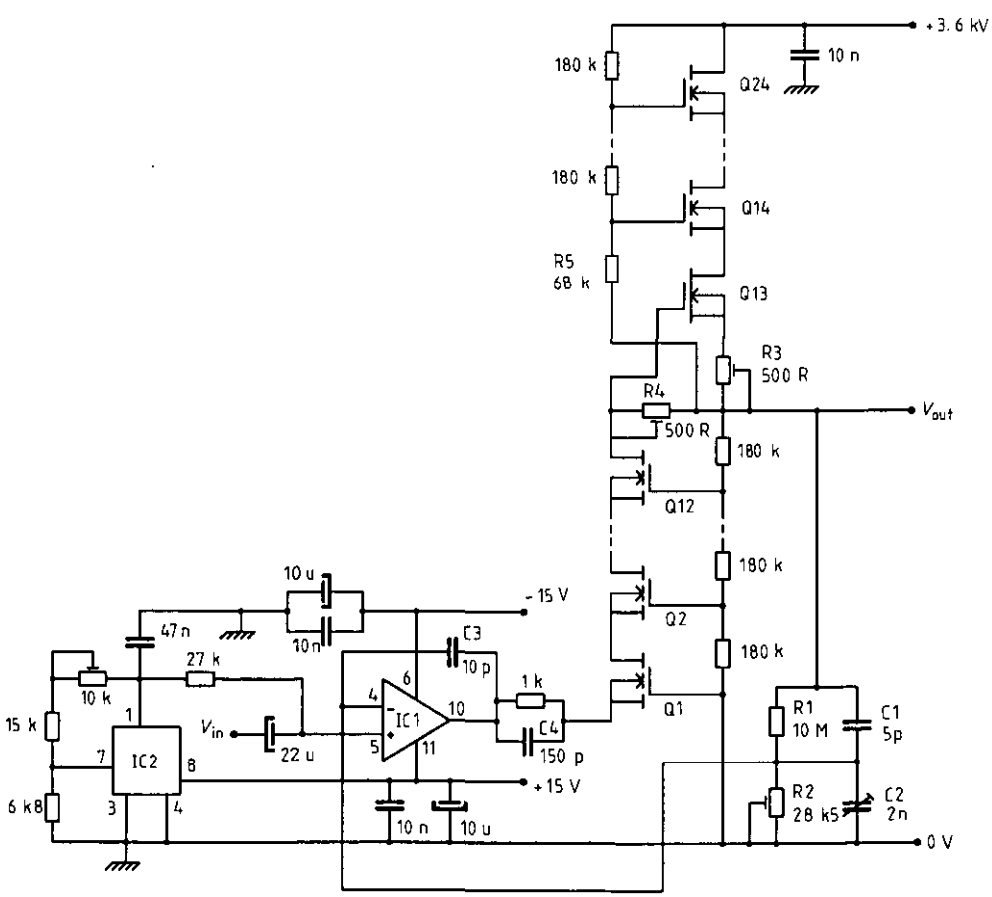

Figure 2. Circuit diagram of high-voltage linear amplifier.

depletion MOSFET, which is biased by the volt drops across the presettable resistors R3 and R4 as discussed later. The enhancement devices Q14 to Q24 serve as self-tracking voltage droppers, ensuring that the drain–gate and drain–source pd values do not exceed 300 V and thus that the average power dissipation per device is below 1 W. Similarly, the current sink comprises Q1 to Q12 and is controlled by the voltage at the op-amp output node.

3.2. Feedback network

A constant fraction of the output voltage is derived from the potential divider R1, C1, R2, C2 and applied to the inverting input of an Analog Devices AD840 high-frequency op-amp (IC1). The choice and adjustment of these feedback components is critical in obtaining optimal amplifier performance. R1 and C1 must withstand the full output voltage, and clearly any variation in their values with voltage will adversely affect linearity and introduce harmonic distortion. A Welwyn T43 series 10 MΩ resistor was found to perform well as R1, having a voltage coefficient of resistance below 10^{-6} V^{-1}. The purpose of C1 in the network is to dominate the stray capacitance distributed across R1 which in practice cannot be adequately compensated by C2 alone. A 5 pF 2.5 kV RF microwave capacitor was used here, it being reasoned that the small dielectric loss in this component would be consistent with a low voltage coefficient of capacitance. To achieve optimum thermal stability, R2 and C2 should both be high-quality components and at least one should be presettable to allow final frequency compensation adjustments to be made. The nominal values given in figure 2 establish a closed-loop voltage gain of 350.

3.3. Stability and compensation

The overall open-loop small-signal response is determined by the product of the transfer functions of the op-amp and the MOSFET ladder stages, including the load impedance. As might be expected, oscillations may occur when the loop is closed unless steps are taken to modify the response in a suitable way. It was found that stability could be achieved under anticipated load conditions by extending the effective bandwidth of the op-amp with the local feedback capacitor C3 and by introducing some phase lead at high frequencies via C4. With the values indicated in circuit a closed-loop bandwidth in excess of 1 MHz could be realized without introducing excessive variations in mid-band gain and phase.

3.4. Current adjustment

Two presettable resistors, R3 and R4, control the current in the upper (source) portion of the MOSFET ladder. R3 sets the self-bias on Q13 and hence the maximum charging current. The voltage drop across R4 depends upon the sink current, and tends to turn Q13 off during a load discharge half-cycle. Thus the overall action of the MOSFET ladder approaches class-B service, with a consequent saving in power. However, in practice it was found that stability and linearity suffer if R4 is too large in value. It should also be pointed out that the negative temperature coefficient of MOSFET threshold voltage renders Q13 susceptible to thermal runaway. For this reason R5 is somewhat smaller in value than the other divider resistors, resulting in a lower average power dissipation in Q13 and minimal warm-up instability.

3.5. Factors affecting output voltage swing

A minimum of some 50 V is required across each half of the MOSFET ladder to maintain saturation, which is an insignificant fraction of the maximum output voltage excursion. The maximum load current which can be handled is somewhat dependent on the instantaneous output voltage, even for a purely capacitive load, owing to the current in the biasing resistors which effectively shunt the MOSFET ladder. With the values used here this amounts to some 1.5 mA at the output voltage extremes in comparison with the output mid-point. While this has no material effect on the large-signal sinewave response, slew-rate limiting on a triangular waveform will occur firstly at the voltage extremes. If the load contains a resistive component then the maximum effective charging current will be further reduced.

The amplifier input is biased to maintain the quiescent output at the mid-point using a National Semiconductors 2951 adjustable voltage regulator (IC2), and is AC coupled to the signal source. This arrangement maximizes the linear output voltage range, and also ensures uniform power sharing between the MOSFETs under both quiescent and driven conditions. When two amplifiers are used in an antiphase bridge, the net DC component across the load may be adjusted either side of zero if required at the expense of a reduced peak-to-peak excursion.

4. Amplifier performance measurement

Measurements of small-signal gain and phase against frequency were carried out using a high-voltage attenuator probe (×1000), oscilloscope and lock-in amplifier. Large-signal linearity and harmonic distortion could not, however, be measured directly, primarily because sufficiently linear and pure signal sources were not available. Instead, the probe output was nulled against an adjustable fraction of the inverted input signal to the amplifier to give a difference signal containing, to first order, only the nonlinearities and harmonics introduced by the amplification process. This signal was displayed on an oscilloscope for linearity analysis, and its second-harmonic component measured using a lock-in amplifier operating in '2f' mode.

For the above measurements to be meaningful it is important that the attenuator probe does not itself corrupt the signal. A home-made probe based on a potential divider similar to the feedback network

described earlier was used here, its output being buffered by an AD847 high-frequency op-amp. When correctly compensated, small-signal frequency response and DC linearity were found to be quite adequate, although no objective means of assessing its large-signal AC performance was available.

5. Results and discussion

5.1. Initial adjustments

In order to obtain optimal charging currents for a given load, and thereby maximize efficiency, R3 and R4 must be set at appropriate values. These adjustments were carried out at a reduced HT voltage (of 1 kV) to avoid excessive dissipation, which requires the DC input bias to be temporarily altered to set the quiescent output at roughly half this value. With R4 initially set to zero, R3 should be adjusted to give a total HT current of about 10 mA, which may then be reduced to the operating level of about 6 mA using R4. The full HT voltage may then be applied and the input bias re-adjusted. It then remains to adjust the feedback components R2 and C2 to obtain optimal frequency response and closed-loop gain. A reasonable setting is achieved by optimising the small-signal square-wave response, although further fine tuning is required for best results under large-signal conditions.

Some difficulties were experienced with instability at low values of load capacitance (below 20 pF). As the load capacitance in the intended application was somewhat larger than this no concerted effort was made to overcome the problem. However, it seems likely that judicious adjustments to C3 and C4 would allow a satisfactory compromise between stability and bandwidth to be achieved under these conditions.

5.2. Small-signal performance

Plots of amplifier voltage gain and phase lag against frequency are shown in figure 3. An input signal of 10 mV peak-to-peak amplitude and total external load capacitance (single-ended) of approximately 50 pF were maintained throughout. It can be seen that the gain varies by only ± 0.5 dB ($\pm 6\%$) about the mid-band value of 50.8 dB up to 1 MHz, peaks by approximately 4 dB at 2 MHz, and then decreases rapidly. These results must be considered quite satisfactory. The phase response displays a lag that is approximately proportional to signal frequency, equivalent to a time delay of some 0.15 μs. This interesting behaviour is probably linked to the multiple parasitic RC elements associated with the MOSFET chain; the consequences with regard to triangular wave amplification are discussed later. Above 2.5 MHz, the phase lag exceeds 180° without oscillation occurring, which must indicate that the feedback network introduces a subtle lead phase-shift sufficient to maintain closed-loop stability.

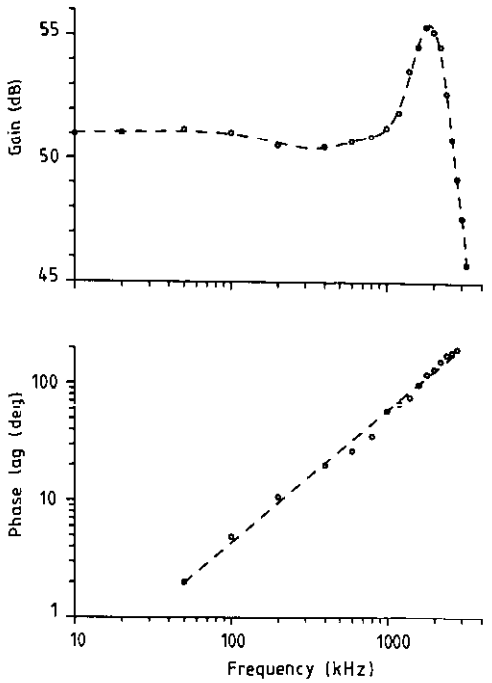

Figure 3. Small-signal voltage gain and phase lag against frequency.

5.3. Harmonic distortion

The harmonic distortion of a sine wave as observed by the nulling method was found to consist predominantly of the second harmonic, it being estimated that the total contribution of third and higher harmonics was at least a factor of five below this. Figure 4 illustrates the approximately frequency-independent parabolic relationship between fundamental and second-harmonic output components, which may be summarized as

$$V(2f)/V(f) = 0.012V(f)\%$$

with $V(f)$ in kV peak-to-peak. Thus, the total harmonic

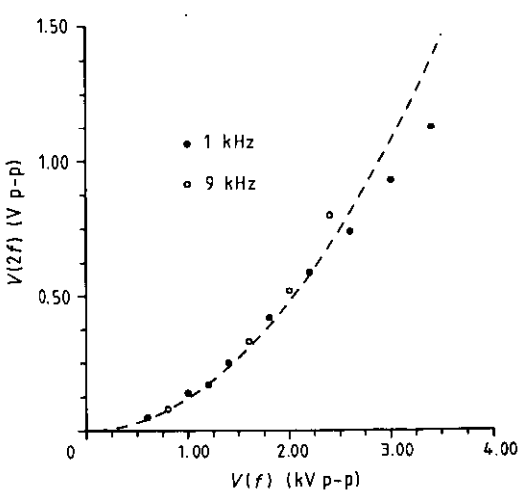

Figure 4. Second-harmonic distortion $V(2f)$ against fundamental output voltage $V(f)$ under sinusoidal input conditions. The broken curve is a parabolic fit to the data. p–p represents peak-to-peak.

distortion at full output (3.4 kV) does not exceed 0.04%. This compares very favourably with the figure of 0.5% quoted for an optically isolated amplifier with lower output voltage capability (Theophanous *et al* 1988) and is quite outstanding by any standards. It must, of course, be recognized that the harmonic content increases dramatically if clipping or slew-rate limiting occur.

5.4. Output drive capability

The frequency f_{SL} at which slew-rate limiting commences for a constant amplitude sine wave $V_0 \sin 2\pi ft$ was investigated as a function of load capacitance in single-ended operation. As

$$dV/dt = 2\pi f V_0$$

and

$$I_0 = (C_0 + C_L)\, dV/dt$$

where C_0 and C_L are the parasitic and external load contributions to the output capacitance, a plot of C_L against $1/f_{SL}$ yields C_0 as intercept, and I_0 may deduced from the gradient. It was found that $C_0 = 14$ pF (the sum of contributions from the MOSFET ladder, feedback capacitor and internal wiring strays), and that the maximum drive current was 8.6 mA. The latter figure agrees well with that expected from the DC settings, and is more than sufficient for the intended application.

For the purpose of considering alternative applications of the amplifier it is instructive to determine the effect of reducing the amplifier supply voltage (and consequently the maximum output swing) and increasing the ladder current settings in the same proportion. This would maintain the same power dissipation while increasing the large-signal bandwidth for a given V_0 and C_L. With the present settings, $I_0 = 8.6$ mA and $V_0 =$ 1.7 kV maximum. On open-circuit output ($C_L = 0$), the total driven capacitance is $C_0 = 14$ pF and f_{SL} for a full-scale sine wave output is calculated to be 56 kHz. With $V_0 = 0.5$ kV, f_{SL} increases to 190 kHz. If, however, the supply is reduced to 1 kV and I_0 increased in proportion we obtain $f_{SL} = 650$ kHz. For a load $C_L = 50$ pF, the above figures become 12 kHz, 42 kHz and 142 kHz respectively. Thus the basic circuit is capable of a large-signal sinusoidal bandwidth of several hundred kHz at 1 kV peak-to-peak output into typical EO loads, with harmonic distortion performance similar to that described earlier, i.e. below 0.01%.

5.5. Triangular wave performance

Difference signals obtained with a triangular wave input at frequencies of 500 Hz and 7 kHz are shown in figure 5. The peak-to-peak output voltages were 3.4 and 3.2 kV respectively into a single-ended capacitive load of 50 pF. At the lower frequency, the difference signal is generated primarily by large-signal nonlinearities, but at the higher frequency phase distortion gives rise to the major contribution. Thus it may be said that the 'dynamic' linearity is poorer at higher frequencies. Expressing this in terms

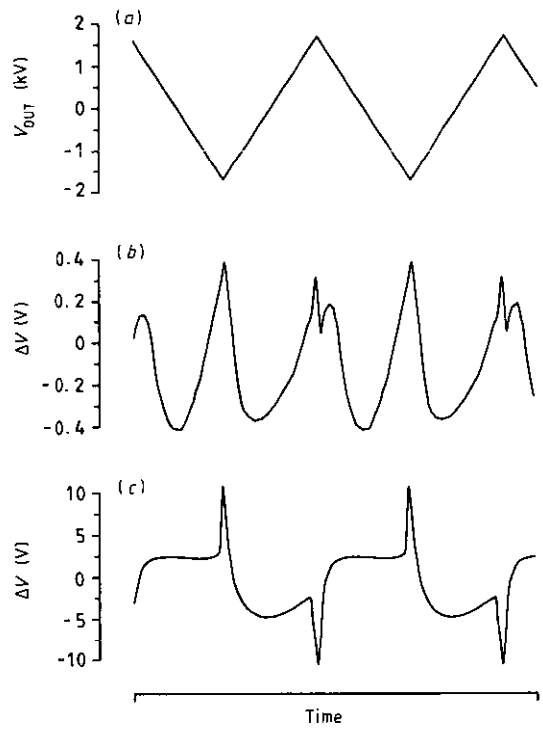

Figure 5. Dynamic linearity performance. Plot (*a*) shows the triangular output waveform on a coarse scale. Plots (*b*) (500 Hz) and (*c*) (7 kHz) represent the difference ΔV between the output obtained in practice and an ideal undistorted output, as described in the text.

of the ratio of the maximum deviation from an ideal triangular output to the total output swing, figures of approximately $\pm 0.01\%$ and $\pm 0.3\%$, respectively, are obtained.

5.6. Temperature stability and noise performance

The temperature stability of gain, frequency response and bias point is governed primarily by the quality of the feedback and biasing components. Very small variations were observed during warm-up, and it is unlikely that such effects would be significant under laboratory conditions provided high-stability components are used. In this respect, performance is much better than amplifiers utilizing optical isolation, where gain coefficients of order 1% $°C^{-1}$ have been reported (Theophanous *et al* 1988).

The quiescent output noise when operating from a well smoothed and filtered HT supply is estimated to be of order 0.01 V RMS, although this figure increased somewhat when a 48 V/3.5 kV switched-mode DC/DC converter was incorporated in the prototype driver.

6. Conclusions

The high-voltage linear amplifier described in this paper can provide a single-ended output voltage of up to 3.4 kV across a capacitive load demanding a charge/discharge current of some 8 mA. Both small and large

signal performance have been investigated in detail. Large-signal harmonic distortion of a sine wave consists primarily of the second harmonic and is below 0.04% at full output, and for a triangular wave a maximum deviation from linearity of $\pm 0.01\%$ is observed at low frequencies (<1 kHz). Higher frequency triangular waveforms are subject to significant phase distortion of high harmonics, which reduces the effective linearity to $\pm 0.3\%$ at 7 kHz into a 50 pF load.

It has been demonstrated that this amplifier offers similar or superior performance in terms of output voltage capability, harmonic distortion, linearity, frequency response, temperature stability and power economy over broadly comparable designs described elsewhere. Although designed specifically as a low-distortion triangular-wave high-voltage driver for an electro-optic crystal load, a potential large-signal bandwidth of several hundred kHz indicates more general applications in high-performance optical systems.

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