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Switching performance of power MOSFETS with capacitive loads at high frequency and high voltage for square wave generators

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Abstract. The limitations of switching capacitive loads between high voltages (1000 V or more) and at high frequencies (10 MHz) using power MOSFETs are discussed. For practical designs, despite the fast rise times of MOSFETs (25 ns), the upper frequency of operation for a specified capacitance and voltage depends mainly on the thermal resistance of the MOSFET. Equations and graphs are presented to show the compromise between load capacitance, required frequency and applied voltage.

Nomenclature

C = Load capacitance
δ = Duty cycle
E = Energy
f = Frequency
FF = Form factor
I = Peak current
i_c = Capacitor current
i_D = Drain current (subscripts 1 and 2 refer to T_1 and T_2)
P = Power (subscripts 1 and 2 refer to T_1 and T_2)
P_{av} = Average power
P_{avp} = Average pulse power
P_p = Peak power
P_{RMS} = RMS power
R = Heat sink thermal resistance
R^1 = Device thermal resistance
R_s = Series output electrical resistance
T = Period
T_1 = Transistor 1
T_2 = Transistor 2
T_a = Ambient temperature
T_c = Case temperature
T_f = Fall time
T_{jmax} = Maximum junction temperature
t_p = Rectangular power pulse duration
T_r = Rise time
V = Supply voltage
v_c = Capacitor voltage
v_{DS} = Drain to source voltage (subscripts 1 and 2 refer to T_1 and T_2)
Z = Transient thermal impedance.

1. Introduction

The advent of high-voltage, fast switching power semiconductor devices has made possible the design of simple and relatively inexpensive instrumentation for generating switched high-voltage waveforms with extremely fast rise and fall times. Such instrumentation has found applications in many areas of current scientific research. One of these applications, electro-rheology, is interesting in that its load is often characterized by being mainly capacitive, thus requiring the switching of large currents during the charge and discharge cycles. Electro-rheology is presently being investigated for its viability in future designs of industrial automotive brakes, clutches, shock absorbers and valves [1, 2]. In these systems the requirement is for high electric fields switched at high frequencies with rise and fall times of less than 1% of the period. The geometry of any practical designs implies that high voltages are required in order to achieve these required electric field strengths. In addition, these applications are typified by their large capacitive load element whereas most power electronic circuits for industrial use, require the switching of inductive (and some resistive) loads.

Different design problems are associated with each

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of the four operating periods of power semiconductor devices, namely turn on, conduction, turn off and off. Most of the heating effects occur during the conduction period while some switching losses, from turn on and turn off also contribute to the heating of a power device. In contrast, the switching of capacitive loads is unusual, with most of the design problems occurring during the turn-on process. During this period, energy is either being stored or removed from the capacitor and the power semiconductor is being heated. The choice of switching device for capacitive loads has been discussed by Bernius and Chutjian [3, 4], who concluded that the power MOSFET is particularly suitable.

There are three basic types of circuit for the application of a voltage square wave to a load capacitor. Figure 1(*a*) shows a unipolar circuit where switching on the top transistor T_1 (with the bottom transistor T_2 off and the capacitor discharged) causes the capacitor voltage v_c to rise to the supply voltage V. Turning off T_1 and turning on the lower transistor T_2 causes the capacitor voltage to fall to zero. This cycle is repeated to generate a repetitive square wave. The output square wave can be varied by raising or lowering the DC supply voltage V, or by changing the operating frequency and mark-to-space ratio of the control electronics (e.g. from a square wave function generator).

When the transistor T_1 is turned on with no initial charge on the capacitor (figure 1(*a*)), the transistor has the full supply voltage across it and provides a current path to charge the capacitor. During this charging period the transistor is dissipating energy and the device junction temperature increases. When the capacitor is fully charged, the transistor has no voltage drop across it and no drain current, so its junction temperature falls until the next time it is switched on. In order not to destroy the device, the junction temperature must not exceed a maximum value which is specified by the manufacturer. The parameters which determine how much power is dissipated by the transistor are the supply voltage, the capacitor size and the operating frequency. An increase in any of these values increases the amount of power dissipated and, hence, the need for a larger heat sink to keep the maximum junction temperature below the upper limit. Also, it seems reasonable that the rise time of the power device, which is limited by its physical properties, has an effect on heating. However, it is shown later that the rise time value is not required for heat sink calculations.

The waveforms for the voltages, currents and powers associated with the circuit in figure 1(*a*) are shown in figure 2. The transistors are assumed to switch on such that the voltages across them rise or fall linearly with time. The turn-off process of each transistor plays no part in the storing or removing of charge from the

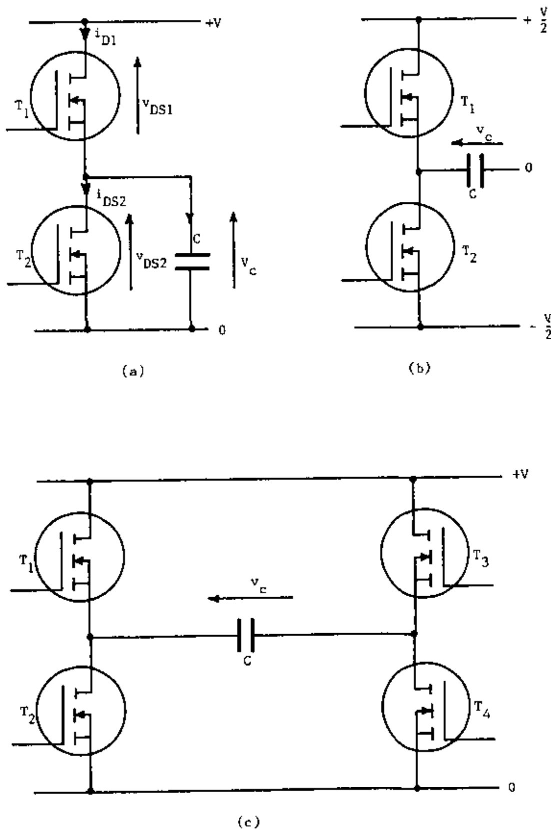

Figure 1. Switching performance of power MOSFETS: (*a*) unipolar circuit; (*b*) bipolar circuit with split supply; (*c*) bipolar circuit.

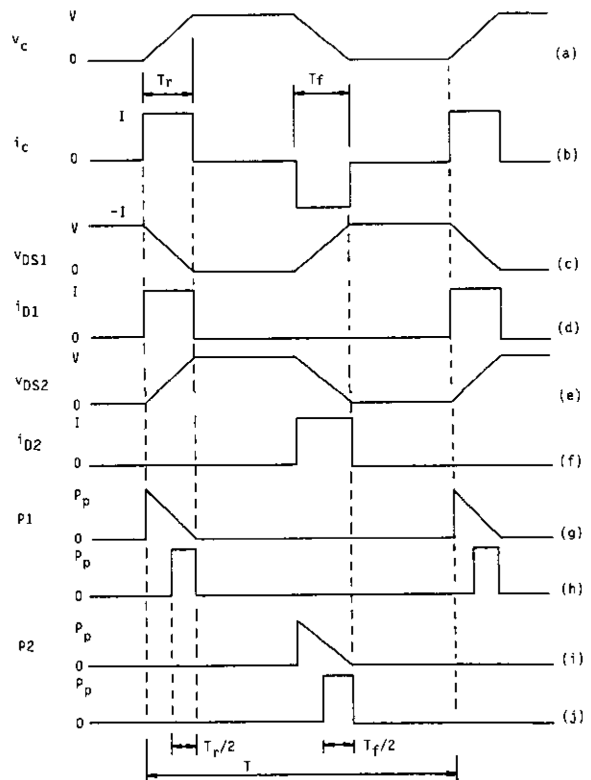

Figure 2. Voltages, currents and powers for the circuit in figure 1(*a*): (*a*) capacitor voltage; (*b*) capacitor current; (*c*) drain–source voltage for T_1; (*d*) drain–source current for T_1; (*e*) drain–source voltage for T_2; (*f*) drain–source current for T_2; (*g*) power dissipated in T_1; (*h*) rectangular power pulse for T_1; (*i*) power dissipated in T_2; (*j*) rectangular power pulse for T_2.

capacitor. The transistors shown in figures 1(*b*) and 1(*c*) are subjected to similar voltages and currents to those shown in figure 1(*a*).

2. Turn on

Assuming that the voltage ramps up linearly with time (figure 2(*a*)), the capacitor voltage v_c during the turn on of transistor T_1 is given by

$$v_c = \frac{Vt}{T_r} \qquad 0 \leqslant t \leqslant T_r \tag{1}$$

where V is the DC supply voltage and T_r is the rise time of the MOSFET.

The capacitor current i_c is given by

$$i_c = C\frac{dv_c}{dt}. \tag{2}$$

Using equations (1) and (2) the peak current and, in this simple case, instantaneous current (figures 2(*b*) and 2(*d*)) is

$$I = \frac{CV}{T_r} \qquad 0 \leqslant t \leqslant T_r. \tag{3}$$

The voltage across the transistor T_1 is given by (figure 2(*c*))

$$v_{DS1} = \frac{V(T_r - t)}{T_r} \qquad 0 \leqslant t \leqslant T_r. \tag{4}$$

The power dissipated in transistor T_1 (figure 2(*g*)) is

$$\begin{aligned} P_1 &= v_{DS1} i_c \\ &= \frac{CV^2(T_r - t)}{T_r^2} \qquad 0 \leqslant t \leqslant T_r. \end{aligned} \tag{5}$$

The average power is

$$P_{av} = \frac{CV^2}{2T} \tag{6}$$

the RMS power is given by

$$P_{RMS} = \frac{CV^2}{(3TT_r)^{1/2}} \tag{7}$$

and the peak power (figure 2(*g*)) is

$$P_p = \frac{CV^2}{T_r}. \tag{8}$$

Using equations (6) and (7) the form factor is

$$FF = 2\left[\frac{T}{3T_r}\right]^{1/2}. \tag{9}$$

Over the rise time T_r the average pulse power is

$$P_{avp} = \frac{CV^2}{2T_r}. \tag{10}$$

Similarly, for the falling part of the waveform during the time T_f, equations (3) to (10) are applicable to the lower transistor T_2. If transistors T_1 and T_2 are the same type of device then the same value of rise time T_r is used for T_f.

3. Power dissipated in the transistors and heat sink specification

The capacitor is charged and discharged during the very short duration of the rise time of each transistor (typically 25 ns). The power dissipated by a transistor peaks at the start of the rise time (figure 2(*g*) and equation (5)). Consequently, the junction temperature of a transistor is 'peaky'. The concept of transient thermal impedance is therefore applicable for the calculation of junction temperature. To determine the device temperature requires that the triangular power pulse (figure 2(*g*)) be converted to a square power pulse having the same energy and peak power as shown in figure 2(*h*). The duration of this equivalent rectangular power pulse t_p is given by

$$\begin{aligned} t_p &= \frac{1}{P_p}\int_0^{T_r} p\,dt \\ &= \frac{1}{P_p}\int_0^{T_r} \frac{CV^2}{T_r^2} t\,dt \\ t_p &= T_r/2. \end{aligned} \tag{11}$$

The transient thermal impedance is given by

$$Z(t_p, \delta) = R'\delta + (1 - \delta)Z(t_p, 0) \tag{12}$$

where R' is the DC thermal resistance of the power device and the duty cycle δ is given by

$$\delta = \frac{T_r}{T}. \tag{13}$$

The duty cycle has a small value since T_r has a small value compared with the period T. Further, $Z(t_p, 0)$ has a small value for a pulse duration of $t_p = T_r/2$.

Approximating, the transient thermal resistance given by equation (12) becomes

$$Z \simeq R'\delta \tag{14}$$

or

$$Z \simeq \frac{R'T_r}{T}. \tag{15}$$

The standard thermal equation is

$$P_p = \frac{T_{jmax} - T_c}{Z}. \tag{16}$$

Combining equations (8), (15) and (16)

$$C = \frac{(T_{jmax} - T_c)T}{R'V^2} \tag{17}$$

or

$$C = \frac{(T_{jmax} - T_c)}{R'V^2 f} \tag{18}$$

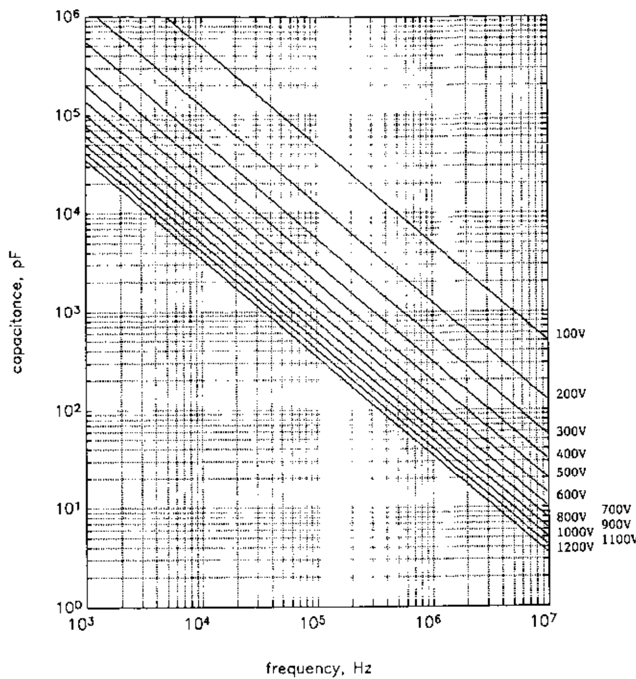

Figure 3. Capacitance against frequency, typical performance.

or

$$\log_{10} C = \log_{10}\left(\frac{T_{jmax} - T_c}{R'}\right) - \log_{10} V^2 - \log_{10} f. \tag{19}$$

The maximum junction temperature T_{jmax} for a MOSFET is typically 150 °C, while the practical limit for a case temperature T_c is about 100 °C [5]. Also, the DC thermal resistance R' is typically $1\ \mathrm{kW^{-1}}$ (range from 0.83 to 6.3). Using these values and for a specified value of voltage, the capacitance plotted against frequency (equation (19)) is shown in figure 3. The lines on this figure show the typical performance for a specified capacitance and voltage. For example, a capacitor of 1000 pF, operating at 1000 V can switch safely at about 50 kHz.

4. Heat sink

While the junction temperature of a MOSFET may be 'peaky', that of the case temperature where the device is attached to a heat sink can be assumed to be constant. This lack of fluctuation in the case temperature is due to the small thermal mass of the power semiconductor compared with that of the heat sink. Average values of variables are therefore used for heat sink calculations. The heat sink equation is

$$P_{av} = \frac{T_c - T_a}{R}. \tag{20}$$

Combining this equation with equation (6) produces

$$\frac{CV^2}{2T} = \frac{T_c - T_a}{R}. \tag{21}$$

For an ambient temperature of 40 °C and a case temperature, as above, of 100 °C, equation (21) becomes

$$R = \frac{60}{Ef} \tag{22}$$

where the energy E is

$$E = \frac{CV^2}{2}. \tag{23}$$

Figures 4(*a*) and 4(*b*) show the energy (equation (23)) plotted for given values of capacitance and voltage. Figure 4(*c*) shows the heat sink thermal resistance as a function of frequency for a given energy (equation (22)). For example, a 1000 pF capacitor operating at 1000 V has an energy of 5×10^{-4} J. A heat sink of about $2\ \mathrm{kW^{-1}}$ is required for operation at 50 kHz.

5. Best performance

Combining equation (21) for the heat sink with equation (17) for the device and eliminating the case temperature variable T_c produces

$$C = \frac{(T_{jmax} - T_a)}{V^2(R' + R/2)f}. \tag{24}$$

Typically the device thermal resistance R' is about $1\ \mathrm{kW^{-1}}$ while the heat sink thermal resistance is small (if the best performance is required). Equation (24) can be approximated to

$$C = \frac{(T_{jmax} - T_a)}{V^2 R' f} \tag{25}$$

or

$$\log_{10} C = \log_{10}\frac{(T_{jmax} - T_a)}{R'} - \log_{10} f - \log_{10} V^2. \tag{26}$$

Using $R' = 1\ \mathrm{kW^{-1}}$, $T_{jmax} = 150$ °C and $T_a = 25$ °C, equation (26) is plotted in figure 5 for values of frequency and voltage. For example, a 1000 pF capacitor operated at 1000 V can achieve 100 kHz switching. The lines on the figure show the upper limits of performance for typical power MOSFETs of a given voltage rating.

6. Discussion and conclusions

At the present time *n*-channel power MOSFETs are capable of withstanding up to 1000 V. Furthermore, at this voltage they are capable of switching about 5 A in 25 ns. This sort of performance suggests that capacitive loads are capable of being switched at 1000 V and 20 MHz. However, the analysis presented in this paper shows that in order to keep the maximum junction temperature below 150 °C requires operation at considerably lower frequencies. For example, a 1000 pF capacitor operated at 1000 V can be switched at only 100 kHz (figure 5). A higher frequency can be achieved using, say, two devices

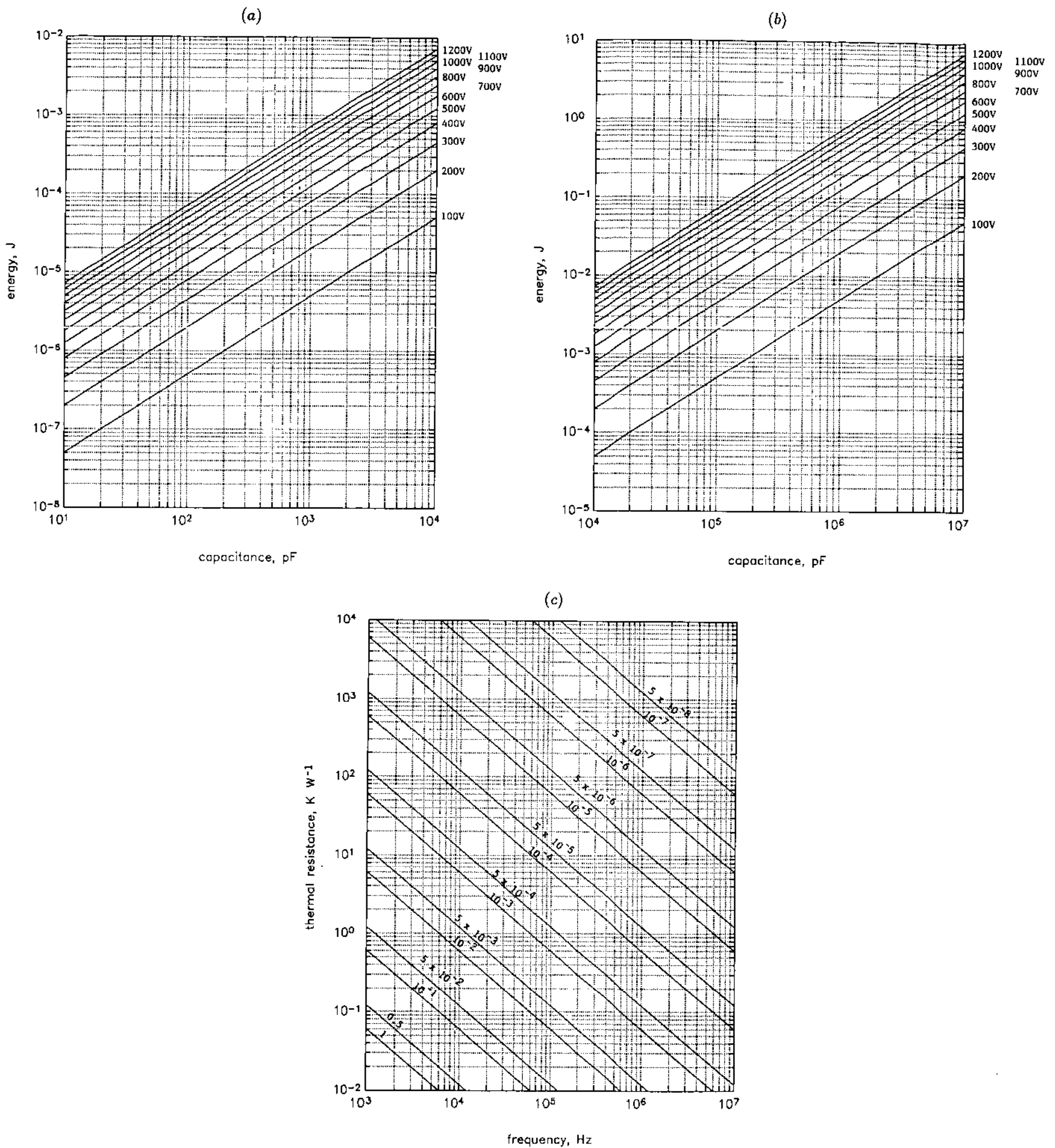

Figure 4. (*a*) Lower capacitances; (*b*) higher capacitances; (*c*) thermal resistance against frequency (entries above lines are energies in J).

in parallel, but this arrangement only allows an increase of a factor of two.

The peak circuit requirement of the DC power supply may add significantly to the cost of the apparatus. This peak current capability can be calculated from equation (3). This value may be large due to the short rise time of a MOSFET. For example, switching a 1000 pF capacitor at 1000 V in 25 ns requires a peak current of 40 A. The peak power required from the power supply is given by equation (8). For the values cited above, a peak power of 40 kW is required. Average and RMS currents and powers are likely to be more manageable. For example, using the values above and operating at 100 kHz requires an average current of 200 mA and an average power of 200 W.

A slower rise time decreases the peak current and power requirements as indicated by equation (3). This slowing may be achieved using a series resistor in the

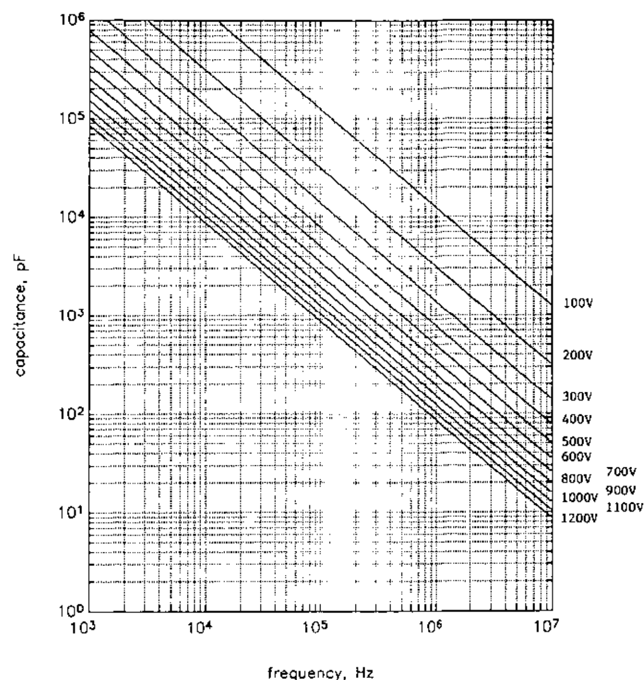

Figure 5. Best performance, capacitance against frequency.

gate circuit thereby creating a low pass filter with the internal gate capacitance of the MOSFET. Slowing the rise time has the benefit of suppressing RF broadcast and reducing any spurious pulses being generated by the low-voltage control electronics associated with the apparatus. Turning off the MOSFET quickly requires a diode to be placed in parallel with the series resistor, thereby providing a low-impedance path to discharge the gate capacitance. If a maximum switching speed is required this practice is not advantageous.

The suppression of noisy pulses in the gate and control electronics requires good UHF construction techniques [2]. In particular, it is desirable that both transistors in the circuit in figure 1(*a*) are not turned on together. If this does occur then the supply is momentarily shorted, creating a large current pulse in the transistors and subsequent overheating [2]. Account has to be taken of the delay times associated with each transistor, delay times through the isolation devices for T_1, and delay times through the control and gate electronics. However it is further possible, due to jitter on the edges of logic circuits, that the occasional short

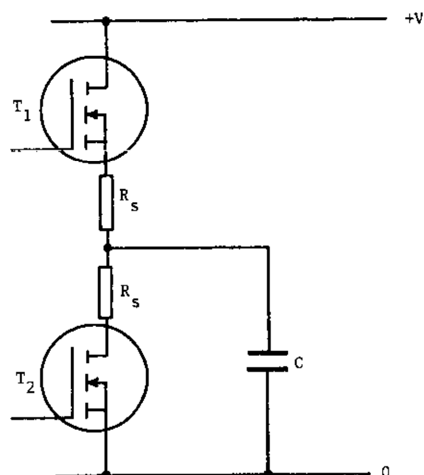

Figure 6. Unipolar circuit with output resistors.

circuit may occur. The circuit shown in figure 6 can overcome this problem successfully. Here the series output resistors allow for a specified short circuit current to occur momentarily without the destruction of the transistors. Most of the power dissipation associated with the charge and discharge of the capacitor, occurs in the resistors and not in the MOSFETS. This circuit has been used successfully for a rise time of 1 μs into a load of 300 pF at 500 V and 10 kHz. Clearly if very short rise times are required then it is not possible to adopt this precautionary measure. The cost of adding the extra resistors is small compared with the benefits and the cost of replacing expensive MOSFETS.

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