# AN1542

# Active Inrush Current Limiting Using MOSFETs

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Input filter design has been an integral part of power supply designs. With the advent of input filters, the designer must take into consideration how to control the high inrush current due to rapid rise of voltage during the initial application of power to the power supply. Depending on the input bus voltage level and the output power required by the load, the supply designer must also design the inductor (if used) to support the DC current without saturating the core. The inductor and capacitor is designed to meet EMI requirements. Limiting initial inrush current with an inductor can become very large in size and weight, and in most cases size and weight is a crucial requirement to the design.

In this section, a review of various active and passive methods of inrush limiting techniques are presented. It is shown that a new and innovative method an be applied using a single MOSFET and a minimal number of components in many of the circuits requiring dv/dt control in order to limit the high current spikes. Its design methods and simple yet effective equations are also presented. A variety of applications of this dv/dt control circuit into other areas are proposed. The simplicity and the advantage of this technique, as opposed to other techniques, is shown given its effectiveness in different applications requiring dv/dt control.

The new inrush limiting is beneficial because dv/dt control reduces the EMI due to current and voltage spikes, and the lifetime of capacitors and the semiconductor devices surrounding the circuitry is increased. This technique will also increase the reliability of the devices and the capacitors. And because of its minimal parts count, the design is very cost effective.

## INTRODUCTION

In power supply designs, the input filter design is an integral part of the design. In most designs input filter designs incorporate both an inductors and capacitors. The inductor and capacitors need to behave in such way as to provide EMI reduction and provide supply hold–up requirement in case of short duration line dropout. This requirement along with derating of the capacitors for temperature variations results in having to use large filter capacitors.

With innovations in technology, the process for manufacturing capacitors allows for very low equivalent series resistance (ESR), and thus they behave like nearly perfect short circuits during initial power application to the power supply [1]. The initial power applied to the power supply posses a very high dv/dt. This high dv/dt interacting with the filter capacitors will introduce short–duration of high peak current which can exceed the device ratings (semiconductor devices, fuses, circuit breakers), and can seriously damage or destroy the semiconductor devices, burn out the fuses or false trigger the circuit breakers. The high rate of rise of the voltage and fast rise of the current may activate other circuitry that are dv/dt and di/dt sensitive. This high dv/dt and di/dt introduces unwanted EMI noise.

It is clear that a new methodology of controlling dv/dt without affecting the inductor size and power supply efficiency needs to be found.

## VARIOUS INRUSH LIMITING TECHNIQUES

Traditionally, most inrush current limiting is done by using a large oversized inductor, or resistors in series with the capacitors. These techniques do not optimally utilize the surface area, weight and power dissipation. In applications where large DC current is required at the input of the power supply, the inductor not only has to be designed for low EMI, but it needs to be designed to meet DC current capability without degrading the inductance value. Reduction in inductance will mean that the EMI noise attenuation capability is reduced. Therefore, the design of inductance becomes very large because with an increase in operating current, the core becomes larger. If a series resistor is used, unnecessary power is lost because of $I^2xR$. This in turn degrades the power supply efficiency. In order to overcome the power dissipation of the series resistor, many designers incorporate a parallel switch with a resistor (semiconductor devices or relays). Depending on the operating current, the relay can become excessively large and heavy. In addition, control circuit must be implemented in order to control the turn–on and turn–off of the relay. In the cases where semiconductors are used, such as an SCR, the device can become very bulky and dissipative. This application also requires unique control circuitry in order to control the SCR turn–on and turn–off.

Another method of inrush current limiting is done using an NTC thermistor. This device has a negative temperature coefficient and its resistance decreases as current is passed through the device (current flow increases the temperature of the device and decreases the resistance) [2]. The drawback of this device is that it requires a "cool off" time after the power is removed in order to reset to high resistive mode. Depending on the power rating of these devices, its physical size becomes significant. The "cool off" time can be overcome by using an active device along with the NTC device. But this defeats the purpose of using the NTC device in the first place; that is, the simplicity of application and minimal parts count.
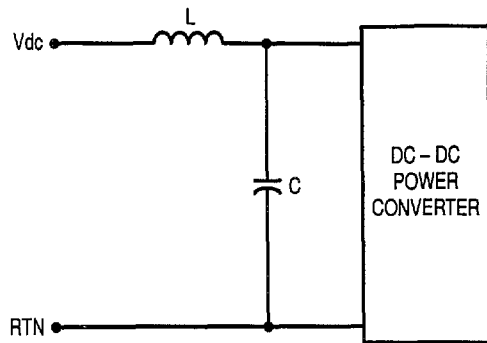
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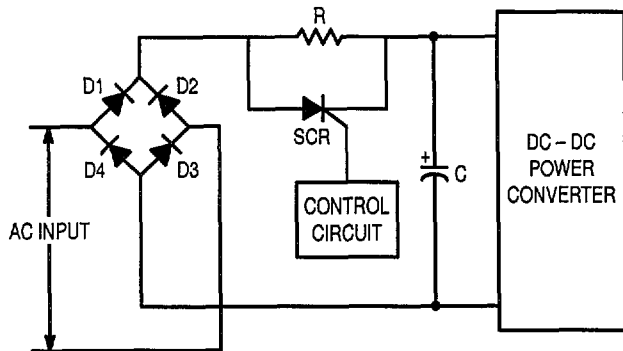
**Figure 1. Inductive**
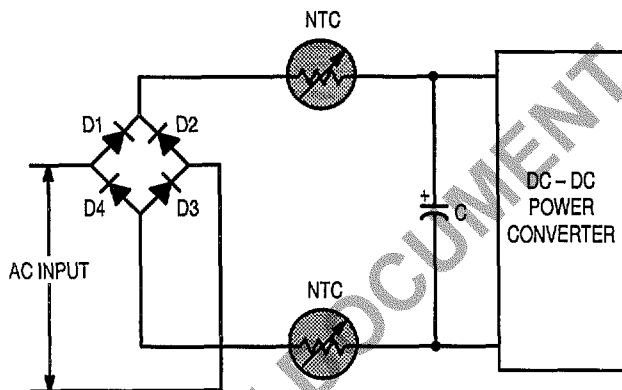
**Figure 2. Passive and Active**

**Figure 3. NTC Thermistor**

## INTRODUCTION TO ACTIVE CURRENT LIMITER

In low to medium power levels which require a few hundred volts of blocking capability, MOSFETs are an ideal devices because they possess the following characteristics: 1) fast switching time due to majority carrier devices, 3) lower switching loss due to fast rise and fall times, 2) simple gate drive, 3) and low $R_{DS(on)}$ which helps to increase the efficiency by decreasing the voltage drop across the device during steady state conduction. Because the active current limiting is done by using MOSFET devices, it is essential that one comprehends the switching characteristics of the devices. By understanding the switching characteristics, the design engineer will be better equipped to use the proposed circuit without any ambiguity.

## MOSFET Switching Characteristics

MOSFETs are charge controlled devices and can be represented with the simplified equivalent circuit shown in Figure 4. The gate–source capacitance ($C_{gs}$) is largely dependent on gate–oxide and source–metallization capacitance and can be measured and considered constant. Gate–drain capacitance ($C_{gd}$) consists of the gate–drain overlap oxide capacitance and gate–drain overlap depletion capacitance. This capacitance is nonlinear due to its voltage dependency. Drain–source capacitance is the depletion capacitance of the drain–source junction. The following expressions can be obtained from the circuit shown in Figure 4.
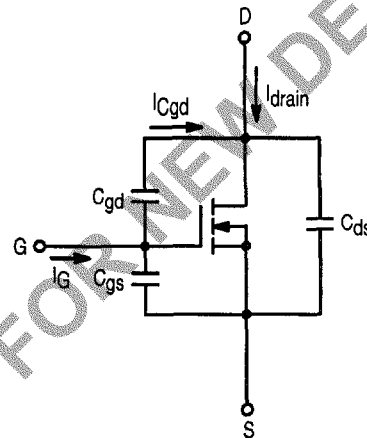
**Figure 4. Equivalent Circuit for MOSFET**

$$C_{iss} = C_{gs} + C_{gd}; C_{ds} \text{ shorted} \qquad (1)$$

$$C_{rss} = C_{gd}, \qquad (2)$$

$$C_{oss} = C_{ds} + \frac{C_{gs} \cdot C_{gd}}{C_{gs} + C_{gd}} ; C_{gs} \text{ shorted} \qquad (3)$$

$$\approx C_{ds} + C_{gd}$$

The expressions shown in equations 1 through 3 are parameters that are available from the MOSFET data sheets and curves provided therein. Capacitance $C_{iss}$ is equivalent input capacitance, $C_{rss}$ is the reverse transfer capacitance, and $C_{oss}$ is the equivalent output capacitance. How fast the capacitance is charged and discharged determines how fast the device will turn–on or turn–off (here the load effect on switching of the device is not considered). The most effective way of obtaining and controlling the switching mechanism of the MOSFET is by using the gate–charge transfer curves as provided by the vendors.

Figure 5 shows the turn–on gate–charge transfer curve. This curve contains all the necessary information for controlling the turn–on switching of the device. Region 1 is a pre–threshold region and the constant current is used to charge the input capacitance $C_{iss}$. During this period, we can ignore the gate–drain capacitance because it is much smaller than the gate–source capacitance and $V_{GS}$ rises to device threshold voltage $V_{th}$ at a linear slope. When $V_{GS}$ has reached the $V_{th}$, the drain current rises to its steady–state drain current during the region. In region 2, the drain–source voltage starts its transition and the gate–charge transfer curve starts to level off.

The slope of the drain–source voltage is much higher in region 2 because the gate–drain capacitance $C_{gd}$ is still relatively small and this small capacitance can be discharged at a faster rate with the given gate current. As the voltage across the drain–gate is reduced even more, the dramatic increase in $C_{gd}$ is observed, and it is this large capacitance which will dominate the input capacitance, and all of the gate current is used to discharge $C_{gd}$. During this flat level (region 3), $V_{GS}$ remains constant, $V_{DS}$ decreases to its saturation voltage, and $V_{sat}$, and the $V_{GS}$ will again rise to its applied gate voltage value. Further increase in $V_{GS}$ has no effect on the drain–source voltage and drain current.
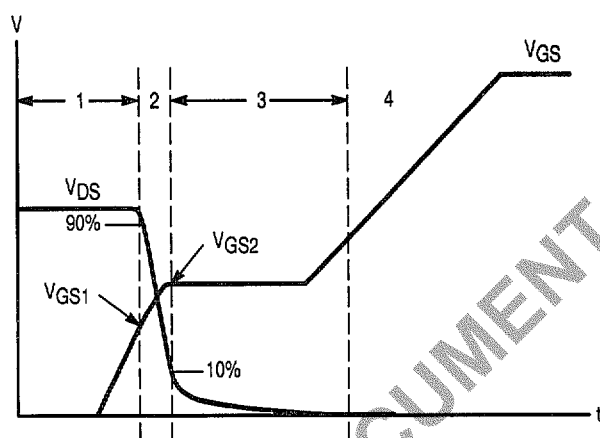


**Figure 5. Gate Charge Transfer Curve**

In observing the gate–transfer curve, it is seen that the $V_{DS}$ transition is determined during region 2 and region 3 of the curve. If the drain–source voltage transition is contained in region 3, it is possible to fix and control the time rate–of–change of the drain–source voltage, $dV_{DS}/dt$, very accurately. The ability for control of region 3 will allow complete control of the $dV_{DS}/dt$ independent of load condition. It is this ability to control $dV_{DS}/dt$ which will allow control of the inrush current to the capacitive load or resistive load.

### Proposed MOSFET Switch

In order to insure that the voltage transition is linear throughout region 3, an external capacitor can be added to the gate–drain connection, $C_{gd}'$. If this capacitance is much larger

than the internal $C_{gd}$, we can rewrite equations 1 through 3 (see Figure 6).
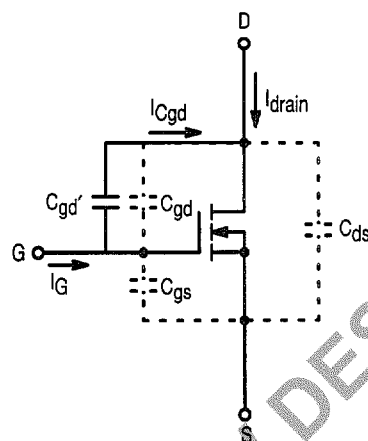


**Figure 6. Revised MOSFET Circuit with External Capacitor**

Given the condition: $C_{gd}' \gg C_{gd}$

$$C_{iss} = C_{gs} + C_{gd} + C_{gd}' \approx C_{gd}' + C_{gs}: C_{ds} \text{ shorted} \quad (4)$$

$$C_{rss} = C_{gd} + C_{gd}' \approx C_{gd}' \quad (5)$$

$$C_{oss} = C_{ds} + C_{gd} + C_{gd}' \approx C_{gd}'; \quad (6)$$

The external capacitance acts as an integrator and is used to accurately determine the switching characteristics of the MOSFET. Its simple expressions allow us to disregard much of the nonlinear capacitive effects of $C_{gd}$ because the capacitance, $C_{gd}'$, along with the gate drive dominates the drain–source voltage transition. The ability to control the constant linear slope of the drain voltage transition allows accurate control of the inrush current to the capacitive load. This is possible because the current flowing through the capacitor is dependent upon the transition of the Voltage:

$$i_c = C \frac{dV}{dt}. \quad (7)$$

### Derivation of the Design Equations for dv/dt Control Circuit

Figure 7 is a circuit used to control the dv/dt of the MOSFET during its switching cycle. $R_G$ is a series gate resistor (which is large in value), and $R_{GD}$ is a small resistor added in series with $C_{gd}'$ to damp out any unwanted high frequency oscillations (this resistor must be much smaller in value than $R_G$: $R_G \gg R_{GD}$. The large value of $R_G$ controls the charge rate of the $C_{gd}'$). The control of the dv/dt is dependent upon the load type and is a function of gate voltage, $R_G$, $V_{DD}$, external feedback capacitance, $C_{gd}'$ and drain current of the device. The diode, $D_g$, is placed in parallel with the $R_G$ to provide faster turn–off process, and can be taken out if slow turn–off is of no concern.
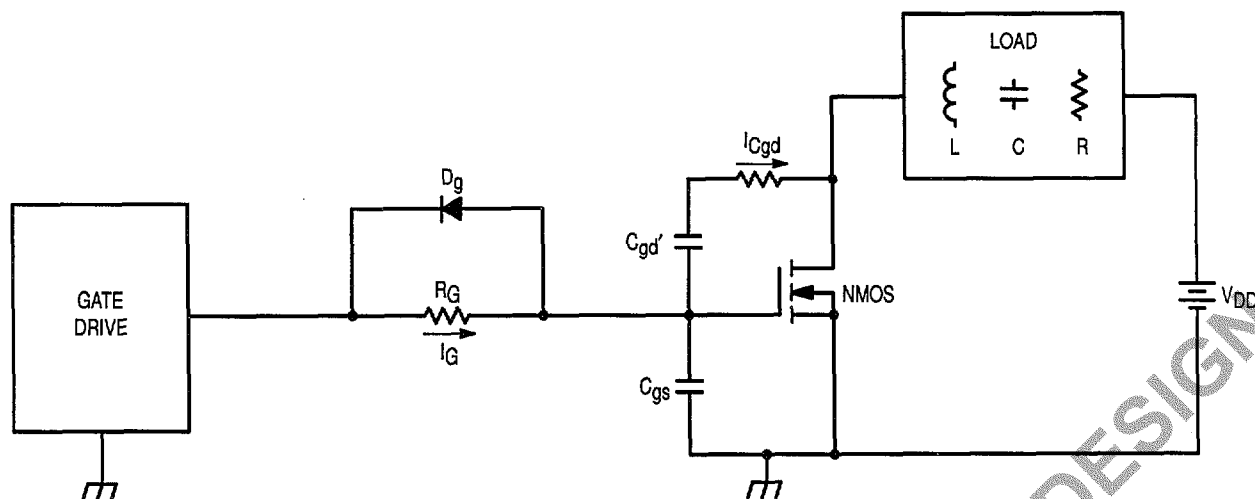
**Figure 7. dv/dt Control Circuit**

Figure 8 is a switching characteristic of dv/dt control circuit of Figure 7, and this curve will be analyzed to derive all of the design equations for the dv/dt circuit.
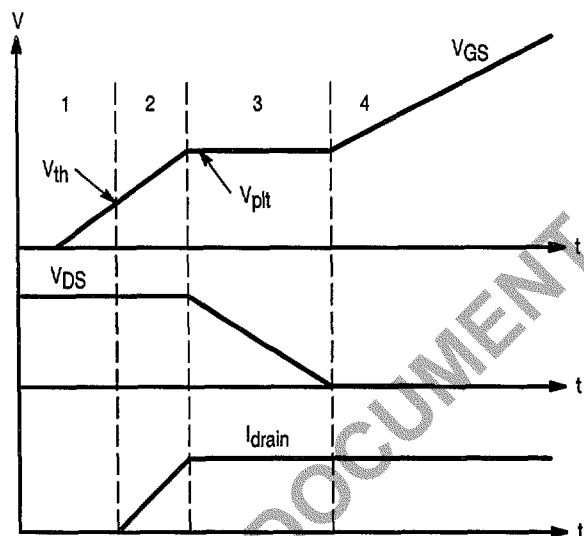


**Figure 8. Gate–Source Charge Characteristic**

### Region 1

During this period, the gate voltage is charging the equivalent input capacitance which is dominated by the feedback capacitance, $C_{gd}'$, expressed in equation 4. This constant capacitance gives constant linear slope, and the gate source voltage will rise exponentially:

$$V_{GS} = V_{GG} [1 - e^{-[t/(R_G(C_{gs}+C_{gd}'))]}] \qquad (8)$$

Turn–on delay is defined as the time required to charge the gate–source to threshold voltage, $V_{th}$. The time delay can be found by using the following equation:

$$t_d = R_G(C_{gs} + C_{gd}') \ln\left|1 - \frac{V_{th}}{V_{GG}}\right|, \qquad (9)$$

### Region 2

Beyond the turn–on delay, region 2, the drain current starts to conduct. The time rate of change of drain current is expressed as:

$$\frac{dI_{drain}}{dt} = g_{fm} \cdot \frac{dV_{GS}}{dt} \qquad (10)$$

Where $dV_{GS}/dt$ is a representation of the slope for regions 1 and 2, and $g_{fm}$ is the transconductance to support the drain current $I_{drain}$. During this time the drain voltage is nearly constant.

### Region 3

In region 3, the transition of the drain–source voltage occurs from its blocking voltage to its saturation voltage once the drain current has reached its maximum load current, and the gate–source voltage remains at plateau voltage $V_{plt}$. Note the difference between Figure 5 and Figure 8. In Figure 8, the transition of drain–source voltage extends **linearly** until the end of region 3. The switching is completed when the drain–source voltage $V_{DS}$ has switched to 10%. Since the drain current is constant during this region, the gate–source voltage (the plateau voltage, $V_{plt}$) must be:

$$V_{plt} = V_{th} + \frac{I_{inrush}}{g_{fm(max)}} \qquad (11)$$

This plateau voltage can be found by using a transfer curve provided by the vendors (see Figure 9).
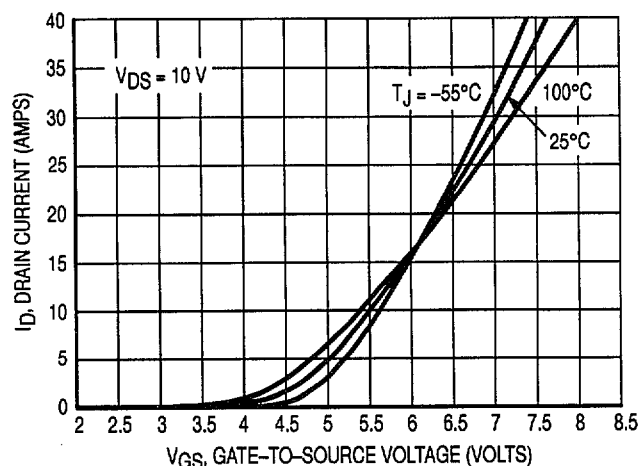


**Figure 9. MOSFET Transfer Characteristics**

The constant $V_{plt}$ allows the input current to flow through the feedback capacitance, $C_{gd}'$, and its current is expressed as:

$$I_g = \frac{(V_{GG} - V_{plt})}{R_G} . \qquad (12)$$

But since the gate current is equal to the current flowing through feedback capacitance, $C_{gd}'$, we can rewrite the above equation as a function of $C_{gd}'$, $V_{DS}$, $V_{plt}$, and time, dt:

Given:
$$I_{gd} \approx I_g,$$
$$I_{gd} \approx C_{gd}' \frac{dV_{DS}}{dt} . \qquad (13)$$

Thus the rate of change of gate–drain voltage is:

$$\frac{dV_{GD}}{dt} = \frac{I_g}{C_{gd}'} = \frac{(V_{GG} - V_{plt})}{R_G \cdot C_{gd}'} . \qquad (14)$$

The time rate of change of drain–source voltage is equal to the time rate of change in gate–drain voltage during the region 3. It is expressed as:

$$\frac{dV_{DS}}{dt} = \frac{(V_{GG} - V_{plt})}{R_G \cdot C_{gd}'} . \qquad (15)$$

**Region 4**

In region 4, the $V_{DS}$ has reached its $V_{sat}$ and $V_{GS}$ continues to increase to its gate voltage, $V_{GG}$.

**dv/dt Design Steps**

The following steps are given in order to simplify some of the equations, and to simplify design procedures.

1. Use equation 7 to find the time required to meet the inrush requirement:

$$dt = C_{filter} \cdot \frac{V_{DD}}{I_{inrush}} . \qquad (16)$$

2. Find the gate–source plateau voltage, $V_{plt}$, required to supply the load current (equation 11). Use the device transfer curve to find the plateau voltage if the data is available.

$$V_{plt} = V_{th} + \frac{I_{inrush}}{g_{fm(max)}} . \qquad (17)$$

3. Choose $C_{gd}'$ based on following condition: $C_{gd}' >> C_{gs} + C_{gd}$ (the values for $C_{gs}$ and $C_{gd}$ is obtained using the data sheet curves).

4. Find the gate current required using equation 13 (the feedback capacitance $C_{gd}'$ is chosen based on availability):

$$I_{gd} \approx C_{gd}' \frac{dV_{DS}}{dt} . \qquad (18)$$

5. Use equation 12 to find the series gate resistance:

$$R_G = \frac{(V_{GG} - V_{plt})}{I_{gd}} . \qquad (19)$$

6. Choose $R_{GD}$: $R_G >> R_{GD}$.

**dv/dt Design Example.** Figure 10 is a test circuit which have been incorporated to test the effectiveness of the circuit. Following parameters were used:

$C_{gs} = 2000$ pF
$V_{DD} = 28$ Vdc
$C_{filter} = 200$ μF
$I_{inrush} = 2$ Apk
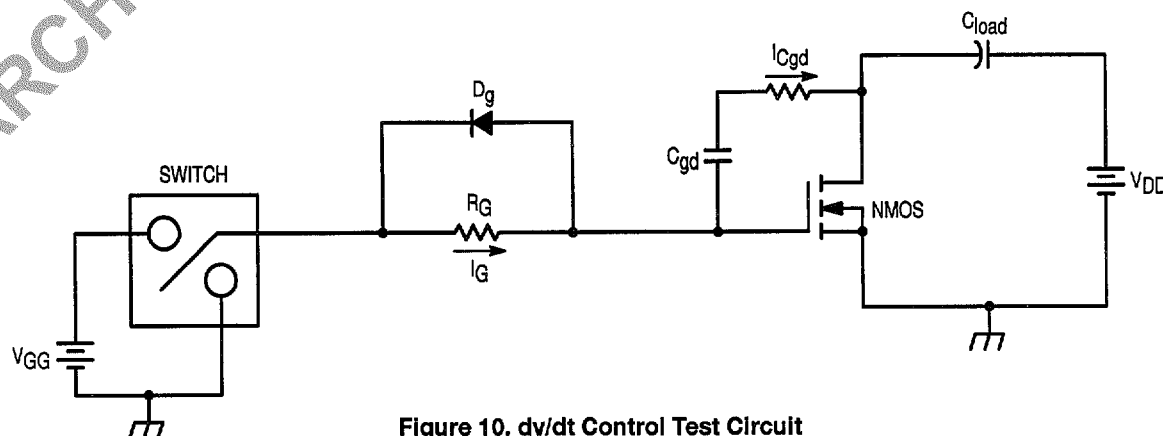$V_{GG} = 12$ V
$V_{th} = 2.7$ V
$g_{fm(max)} = 2.5$ S



**Figure 10. dv/dt Control Test Circuit**

### Step 1

Using the expression i = C(dv/dt), the transition time for $V_{DS}$ is found:

$$dt = C_{filter} \cdot \frac{V_{DD}}{I_{inrush}} = 200 \ \mu F \ \frac{28}{2} = 2.8 \ ms \qquad (20)$$

### Step 2

During the $V_{DS}$ transition, $V_{GS}$ is constant and equation 11 is used to find the $V_{plt}$ for desired peak drain current (use the transfer curve if available).

$$V_{plt} = V_{th} + \frac{I_{inrush}}{g_{fm(max)}} = 2.7 + \frac{2}{2.5} = 3.5 \ V. \qquad (21)$$

### Step 3

Satisfying the condition $C_{gd}' \gg C_{gs} + C_{gd}$, 0.1 $\mu F$ was arbitrarily chosen. We can either choose initial value of $R_G$ or $C_{gd}'$, and design for the unknown. But in most cases, different values of resistor is easier to obtain than the capacitors. So for this design example, $C_{gd}'$ was chosen.

### Step 4

Use equation 14 to find required gate current:

$$I_{gd} \approx C_{gd}' \ \frac{dV_{DS}}{dt} \approx 0.1 \ \mu F \ \frac{28}{2.8 \ ms} \approx 1 \ mA. \qquad (22)$$

### Step 5

Using the calculated values from 21 and 22, series gate resistor is calculated:

$$R_G = \frac{(V_{GG} - V_{GS})}{I_{gd}} = \frac{(12 - 3.5)}{1 \ mA} \approx 8.5 \ k\Omega. \qquad (23)$$

### Step 6

The damping resistor can be chosen arbitrarily if the following condition is met:

$$R_G \gg R_{GD},$$

Let $R_{GD} = 100 \ \Omega.$

### di/dt Design

In some cases the initial rate of rise of the drain current must be limited to some fixed rate. The current slope limiting reduces transients associated with L(di/dt) due to stray inductances. This current slope limiting reduces the problem of loading of the line which can cause a temporary line dropout [3].

We can determine from the Figure 11 that **time for $V_{GS}$ to reach a voltage level given by equation 11 must be greater than the sum of delay time, $t_d$, and the time required for drain current to reach steady state value:**

$$t_{Vgs} > t_d + dit. \qquad (24)$$

Where $t_{Vgs}$ is the time required for $V_{GS}$ to reach a value that will support the inrush current obtained by equation 17, and $I_{inrush}$ is the maximum inrush current flowing through the MOSFET.
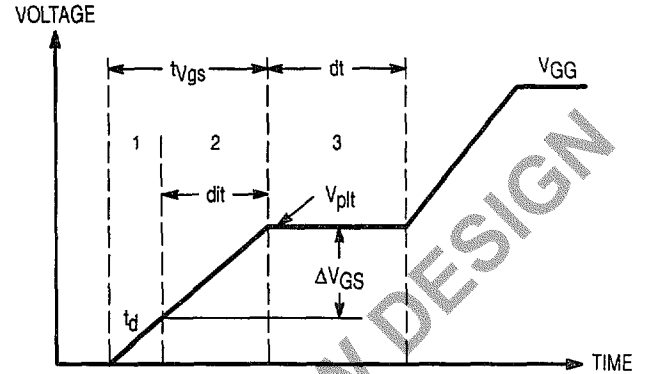


**Figure 11. Expanded View of Gate–Source Voltage**

The rate of rise time of the drain current of the device is directly proportional to the rate of rise of the gate–source voltage (see equation 10):

$$\frac{dI_{drain}}{dt} \propto \frac{dV_{GS}}{dt} \qquad (25)$$

The rate of change of drain current is a design requirement. As a result, we can find the minimum time required for gate–source voltage to reach the value to support the initial inrush current:

$$t_{Vgs(min)} = \frac{V_{plt}}{(dI_{inrush}/dt)}. \qquad (26)$$

Using the minimum time required, the following must be satisfied:

$$R_G \cdot (C_{gs} + C_{gd}') \geq \frac{-t_{Vgs(min)}}{\ln \left| 1 - \dfrac{V_{plt}}{V_{GG}} \right|}. \qquad (27)$$

If the above expression is not satisfied, then one of the parameters ($R_G$ or $C_{gd}'$) must be changed to satisfy the equation.

**di/dt Design Example.** For the same circuit used for dv/dt control, the following current requirement must be met:

$$\frac{dI_{drain}}{dt} = \frac{2A}{100 \ \mu s}. \qquad (28)$$

### Step 1

The minimum time required is:

$$t_{Vgs(min)} = \frac{3.5}{(2 \ A/100 \ \mu s)} = 175 \ \mu s. \qquad (29)$$

**Step 2**

Once total time required is calculated, the time constant can be checked (the effect will be discarded):

$$RG \cdot (C_{gs} + C_{gd}') = 8.5K \cdot (2000 \text{ pF} + 0.1 \text{ } \mu F) = 867 \text{ } \mu s. \tag{30}$$

and,
$$\frac{-tV_{gs(min)}}{\ln\left|1 - \dfrac{V_{plt}}{V_{GG}}\right|} = \frac{-175 \text{ } \mu s}{\ln\left|1 - \dfrac{3.5}{12}\right|} = 507 \text{ } \mu s. \tag{31}$$

Thus

$$RG \cdot (C_{gs} + C_{gd}') \geq \frac{-tV_{gs(min)}}{\ln\left|1 - \dfrac{V_{plt}}{V_{GG}}\right|} = 867 \text{ } \mu s \geq 507 \text{ } \mu s. \tag{32}$$

The condition is satisfied and nothing needs to be changed. If equation 32 was not satisfied, a different value of $R_G$ (or $C_{gd}'$) can be chosen.

## CONCLUSION

It is shown in this section that by using a low $R_{DS(on)}$ MOSFET in current limiting, the shortcomings due to passive methods can be overcome. Using a MOSFET device in an active dv/dt and di/dt control is useful due to the simple gate drive requirements and low $R_{DS(on)}$. With just a single MOSFET and its corresponding components, dv/dt and di/dt transition can be accurately controlled. This control circuit results in precise control of inrush current magnitude, and reduces much of high frequency noise associated with high voltage and current transitions. Not only is the circuit precise, but it also reduces weight and surface area as opposed to bulky inductors.

The simple and yet effective equations have been derived for dv/dt and di/dt control circuit. These simple equations with appropriate components can overcome even some of the most stringent inrush current limiting requirements without sacrificing weight and area. The following are the design objectives which have been discussed:

1. Add a feedback capacitance $C_{gd}'$ to negate the nonlinear voltage dependent capacitor $C_{gd}$.
2. The following requirement must be met: $C_{gd}' >> C_{gs} + C_{gd}$ (maximum $C_{gd}$ can be obtained from the vendor data).
3. Linearize the rate of change of drain source voltage during all of the active region (region 3).
4. Control $dV_{DS}/dt$ by controlling the charge rate of $C_{gd}'$.
5. Fix the charge rate by controlling the charging current.
6. Gate current $I_G$, is fixed during active region by choosing correct $R_G$.

# APPLICATIONS USING DV/DT CONTROL CIRCUIT

### INTRODUCTION

The active dv/dt circuit is applicable to many applications which require slow ramp up of voltage across the load or current through the load. Detailed analysis was done in previous section of the paper which showed all of the required design equations. Using these same equations, and with slight modifications, dv/dt circuit can be implemented to numerous applications. In this section some examples will be shown and discussed where it is appropriate.

### Series Pass Switch

There are requirements where the power to the load must be switched on at a controlled rate either 1) due to inrush current requirement to capacitive load or 2) due to power source type (batteries). Using a MOSFET to switch on the power to the load allows the flexibility of accurately controlling the dv/dt and di/dt to the load. Using a controlled ramp–up of power to the load also relaxes some of the load transient requirements for primary power source (DC–DC SMPS).

The following examples are circuits used for switching power to the load. The examples are given to show how the different device types can be implemented in a switching load application using the dv/dt concepts discussed previously. The same design steps can be followed as in previous sections. But for simplicity, all the steps will be rewritten for the convenience of the reader.

### PMOS Application

Given: output voltage transition time dt,
output voltage, $V_{out}$
gate voltage, $V_{GG}$
gate drain capacitance, $C_{gd}'$
gate–source plateau voltage, $V_{plt}$

1. Choose $C_{gd}' \gg C_{gs} + C_{gd}$

2. $I_{gd}' \approx C_{gd}' \dfrac{dV_{DS}}{dt} = C_{gd}' \dfrac{V_{out}}{dt}$     (1)

3. $R_G = \dfrac{V_{DD} - V_{plt}}{I_{gd}'}$ or     (2)

$R_G = \dfrac{V_{DD} - V_{plt}}{I_{gd}'}$: if very low output current (in mA).     (3)
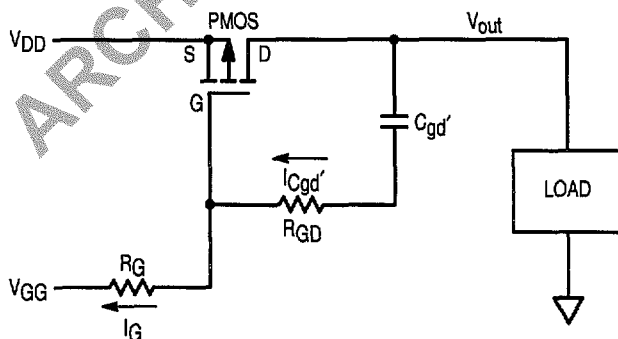
Choose $R_{GD} \gg R_G$.



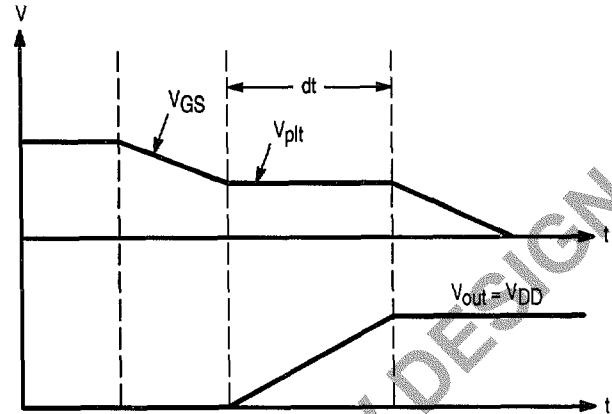**Figure 1. dv/dt Control Circuit Used As Load Switch**



**Figure 2. PMOS Switching Transitions**

### NMOS Application

When NMOS is used to switch the power to the load, the gate voltage of the device is constantly increasing nonlinearly due to the output voltage level shifting the gate–source voltage, $V_{GS}$ (see Figure 4).
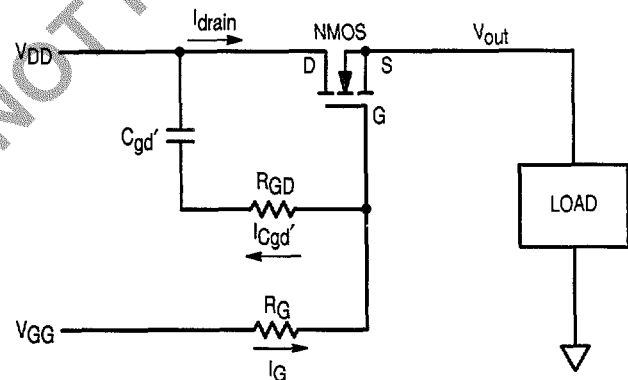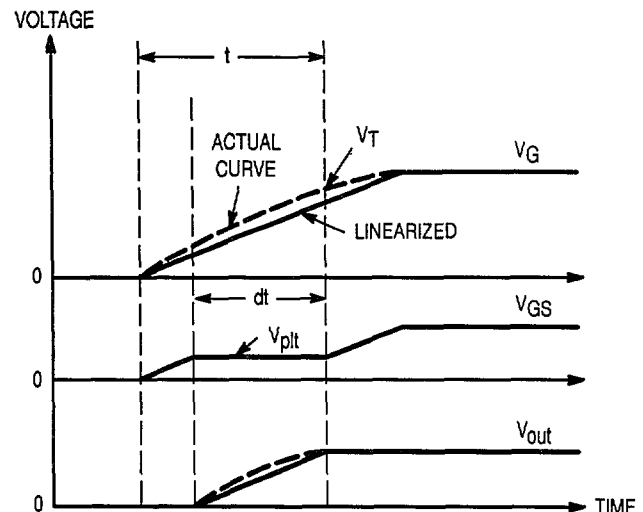


**Figure 3. NMOS Load Switch**



**Figure 4. Voltage Transitions of NMOS Switch**

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The gate voltage is changing at a rate:

$$V_G = V_{GG} \left(1-e^{-(t/R_{GD}C_{gd}')}\right) \quad (4)$$

Note that gate voltage has to be greater than the input dc voltage; $V_{GG} > V_{DD}$. Taking this assumption we can then linearize the gate voltage curve and the following design requirements be implemented:

1.  Choose $C_{gd}' \gg C_{gd} + C_{gs}$

2.  Find the gate voltage at which the output will have ramped up to its input voltage:

$$V_T = V_{plt} + V_{out} \quad (5)$$

3.  Find the total time required for gate voltage to reach $V_T$.

$$\frac{V_{out}}{V_T} = \frac{dt}{t}, \quad (6)$$

and 

$$t = dt \, \frac{V_T}{V_{out}}, \quad (7)$$

where, t, is equal to time needed for gate to charge up to $V_T$.

4.  Calculate the series gate resistor using the time, t:

$$R_G = \frac{-t}{C_{gd}'} \cdot \frac{1}{\ln\left|1 - \dfrac{V_T}{V_{GG}}\right|} \cdot \quad (8)$$

Choose $R_{GD} \ll R_G$.

**Sample Calculations:**

Given:

$V_{DD} = 5\ V$
$V_{out} = V_{DD} = 5\ V$
$V_{GG} = 12\ V$
$dt = 5\ ms$
$V_{plt} = 2.7$

1.  $C_{gd}' = 0.1\ \mu F \quad (9)$

2.  $V_T = V_{plt} + V_{out} = 2.7 + 5 = 7.7 \quad (10)$

3.  $t = dt \, \dfrac{V_T}{V_{out}} = 5\ ms \, \dfrac{7.7}{5} = 7.7\ ms \quad (11)$

4.  $R_G = \dfrac{-t}{C_{gd}'} \cdot \dfrac{1}{\ln\left|1 - \dfrac{V_T}{V_{GG}}\right|} = \dfrac{-7.7\ ms}{0.1\ \mu F} \cdot \quad (12)$

$\dfrac{1}{\ln\left|1 - \dfrac{7.7}{12}\right|} = 75\ k\Omega$

2.  Let $R_{GD} = 100$

## INRUSH CURRENT LIMITER FOR DC–DC CONVERTERS

Figures 5a and 5b shows the dv/dt circuit used as a inrush current limiter in a DC–DC power converter (The operation of the circuit is not discussed in this section, but is presented in the following section). In Figure 5a, the MOSFET is placed in the return path of the power supply. This will cause the SMPS RTN path to rise to the $V_{DD}$ value, and then it is brought down to ground potential at a fixed rate by the dv/dt control circuit. This configuration is beneficial where the $R_{DS(on)}$ of the MOSFET does not introduce an additional ESR to the filter capacitor.

Figure 5b shows the dv/dt circuit placed in series with the input filter capacitor. This configuration is beneficial because the MOSFET can never be shorted due to improper ground connection, and the $R_{DS(on)}$ can act as an damping resistor.
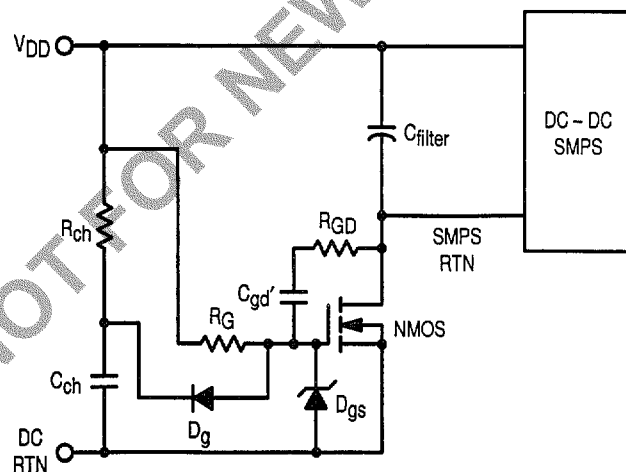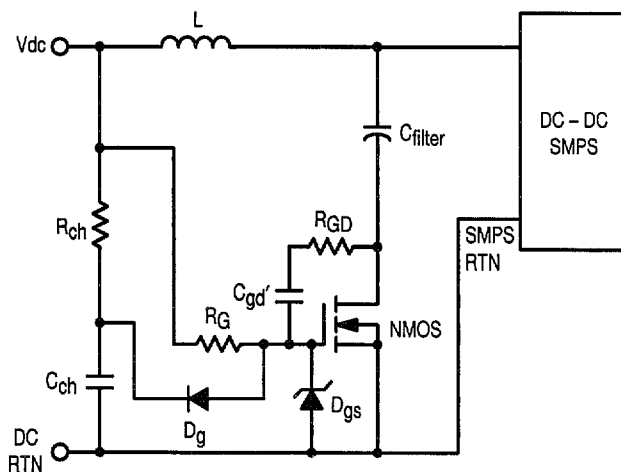
**Figure 5a. MOSFET Placed at Return Path**

**Figure 5b. MOSFET Placed Series With Filter Capacitor**

## INRUSH CONTROLLER FOR DC LIGHT BULBS

In order to prolong the lifetime of Incandescent lamps, the inrush current must be controlled (it can be any light emitting device). If many light bulbs are paralleled, the peak current to the load must be controlled because it may exceed the fuse or circuit breaker rating. By using the dv/dt controlled circuit, the inrush current can be controlled accurately. Initially the light bulb has very low cold resistance, but once the current is conducting the filament warms up and its resistance increases accordingly. The dv/dt control circuit is used so that the voltage across the lamp will increase very slowly, and this slow rise of the voltage will allow the lamp to heat up before the full supply voltage is across the lamp.
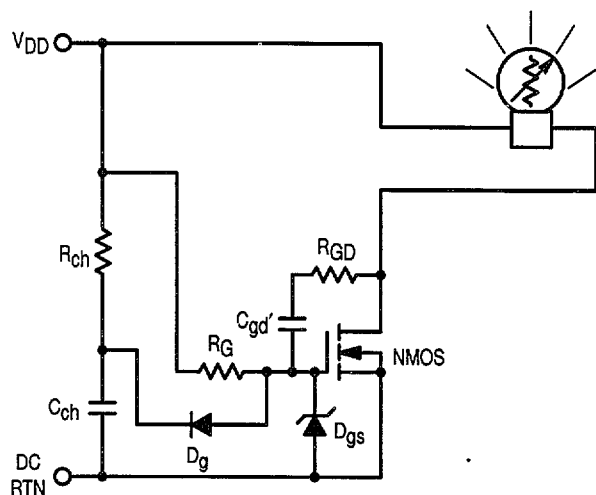


**Figure 6. Inrush Limiter for Incandescent Light Bulbs**

## CONCLUSION

Active dv/dt control circuit can be applied to numerous applications where voltage and current must be controlled at initial turn–on. It was shown in this section that the circuit can be implemented in series switch to the load, control input filter inrush current, and control inrush current to the dc light bulbs. Using dv/dt control circuit is beneficial because it reduces the EMI and prolongs the lifetime of the electronic components in the circuit.

# AVOIDING FALSE TURN–ON DUE TO STATIC DV/DT FOR MOSFET–BASED ACTIVE INRUSH CURRENT LIMITER

Figure 1 is a active inrush current limiter incorporated into DC–DC power converter. Initially the NMOS switch is turned off until the dc bus voltage $V_{DD}$ is applied. In many applications, the input voltage $V_{DD}$ is switched. The rate of rise of the supply voltage is a function of the switch speed and the parasitic components within the circuit. When $V_{DD}$ is fully applied to the circuit, the drain of the MOSFET will see all of the applied voltage because of its high impedance during its off state. When high dv/dt is applied to the drain of the MOSFET, the voltage transient can be fed back to the gate via drain–gate feedback capacitance. If there is enough charge present in the gate, the switch will turn on and the dv/dt control will be lost. The magnitude of the gate–source voltage will depend upon the gate–impedance of the device.
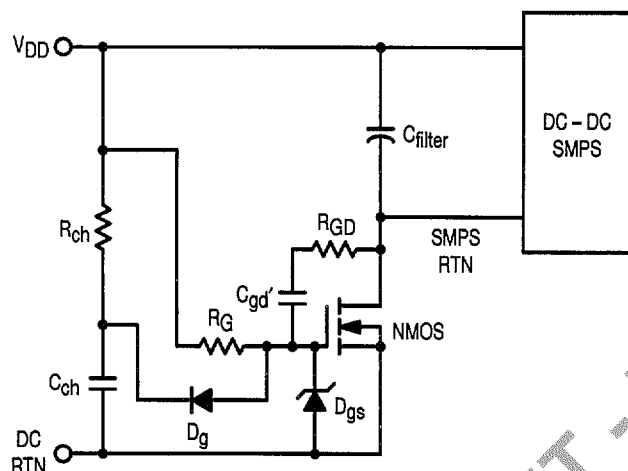


**Figure 1. Inrush Current Limiter**

Figure 2 is a equivalent circuit for MOSFET showing the internal parasitic capacitance. In order to show how much impact the parasitic capacitance has during initial voltage applied to the drain of the device, consider the following example.

Given:
$C_{gd}$ = 200 pF
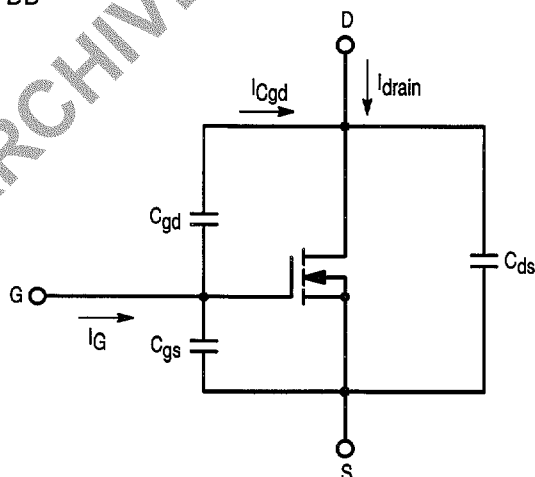$C_{gs}$ = 2000 pF
$V_{DD}$ = 100 V



**Figure 2. MOSFET Equivalent Circuit**

We will assume the worst case (step function). When $V_{DD}$ is applied, the instantaneous gate–source voltage will charge up to the following:

$$V_{GS} = V_{DD} \frac{C_{gd}}{C_{gs} + C_{gd}} = 100 \frac{200}{200 + 2000} = 9.1 \text{ V}. \quad (1)$$

This voltage is high enough to turn the device fully on and cause a large inrush current to flow through the input filter capacitance. In Figure 1 the capacitance $C_{ch}$ is inserted in order to keep the $V_{GS}$ at a level below the threshold voltage, and keep the device off during step voltage application.

Figure 3 shows the representation of the time varying voltage and current waveforms for the circuit shown in Figure 1. During the initial application of the voltage, the gate voltage will try to ramp up because of high dv/dt seen via the feedback capacitance $C_{gd}'$, but as soon as the gate–source voltage is high enough to turn the diode $D_g$ on, it causes all of the charge to be transferred to capacitance $C_{ch}$. The voltage across the charge capacitance $C_{ch}$, is determined by the voltage division between $C_{ch}$ and $C_{gd}'$. This voltage across the charge capacitance is expressed as:

$$V_{ch} = V_{DD} \cdot \frac{C_{gd}'}{C_{gd}' + C_{ch}}. \quad (2)$$

The capacitance $C_{ch}$ must be large enough in order to maintain the device in the off state. The gate–source voltage will be:

$$V_{GS} = V_{ch} + V_{DG}, \quad (3)$$

where $V_{DG}$ is a junction potential of the diode $D_g$.
Initially, the current flowing through the $R_{GD}$, and $C_{gd}'$ is:

$$i_o = \frac{V_{DD}}{R_{GD}}, \quad (4)$$

and this current decays exponentially at a rate:

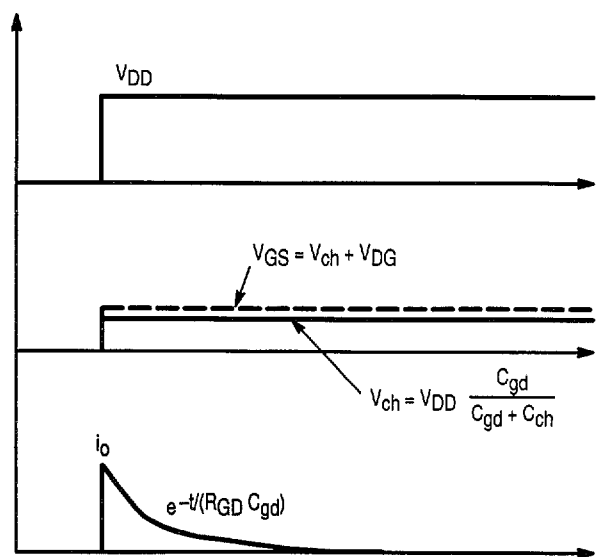$$i_{Cgd}' = i_{Rgd} = i_o e^{-t/(R_{GD} \cdot C_{gd}')} \quad (5)$$



**Figure 3. Step Function**

During the step voltage application, the voltage across $C_{ch}$ is set at:

$$V_{ch} = Vth_{min} - V_{DG} = Vth_{min} - 1. \qquad (6)$$

This is to insure that the MOSFET does not turn on during the initial $V_{DD}$ application.

In Figure 3, it is shown that the initial current during the step function is determined by the $R_{GD}$ and $V_{DD}$. This current than decays at some exponential rate. In order for the $V_{GS}$ not to overshoot, the time delay must be provided by the $R_{ch}C_{ch}$ time constant such that the gate–source voltage must not rise to $V_{plateau}$ before the current has decayed to near zero. If $V_{GS}$ has reached plateau voltage $V_{plt}$, before the current has decayed to zero, a overshoot will be observed at the gate and the device will turn on rapidly for a short duration and may cause excessive inrush current to flow through the input filter capacitor, $C_{filter}$.

### Operation of Charge Control Circuit

Figure 1 is an equivalent circuit for an inrush current limiter. When $V_{DD}$ is applied, the charge capacitance maintains the $V_{GS}$ to a safe level so that the MOSFET does not turn–on. The capacitance $C_{ch}$ is then charged at a rate dependent on ($R_{ch} \cdot C_{ch}$) time constant, and $V_{GS}$ charges at the same rate (at diode drop greater) until it reaches a voltage to support the inrush current. The drain voltage decreases at a linear slope which is determined by the ($R_G \cdot C_{gd}'$) time constant. This slope then determines the maximum magnitude of the inrush current to the capacitors. Examples of the theoretical waveforms are shown in Figure 4.
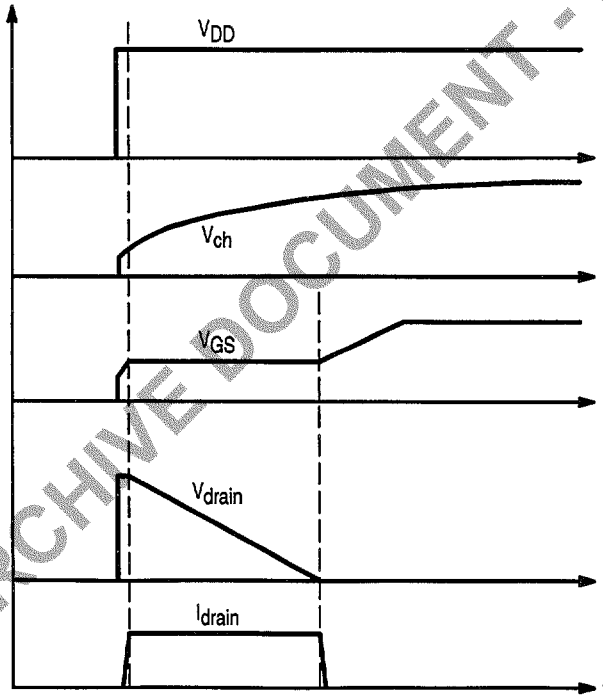


**Figure 4. Switching Waveforms**

### Design Equations

The total decay time required for the initial current is found by taking equation 5 and solving for time, t:

$$t_{delay} = R_{GD} \cdot C_{gd}' \cdot abs \ln \left| \frac{i_{Cgd'}}{i_o} \right|, \qquad (7)$$

where $i_{Cgd}'$ is the current through the feedback capacitance at given time. For this purpose, the desired current level is set at 0.5% of initial current $i_o$. The time delay is than expressed as a function of feedback resistor $R_{GD}$, and capacitance $C_{gd}'$:

$$t_{delay} \approx 5.3 \, R_{GD} \cdot C_{gd}' \qquad (8)$$

where the constant 5.3 is obtained by:

$$abs \ln \left| \frac{i_{Cgd'}}{i_o} \right| = abs \ln |0.005| \approx 5.3. \qquad (9)$$

The time constant $R_{ch}C_{ch}$ must meet the following condition:

$$R_{ch} \cdot C_{ch} \geq \frac{t_{delay}}{abs \ln \left| 1 - \dfrac{(V_{plt} - V_{ch} - V_{DG})}{V_{DD}} \right|} \qquad (10)$$

where, $V_{ch}$ is found by using equation 6.

The capacitance $C_{ch}$ is found using the following expression:

$$C_{ch} \approx \frac{C_{gd}' \cdot (V_{DD} - V_{ch})}{V_{ch}} \qquad (11)$$

and charge resistance, $R_{ch}$ is:

$$R_{ch} \geq \frac{1}{C_{ch}} \cdot \frac{t_{delay}}{abs \ln \left| 1 - \dfrac{(V_{plt} - V_{ch} - V_{DG})}{V_{DD}} \right|} \qquad (12)$$

### Design Steps for Charge Control

When designing for the $C_{ch}$ and $R_{GD}$, following steps must be done in order:

1. Find the voltage $V_{ch}$:

$$V_{ch} = Vth_{min} - V_{DG} = Vth_{min} - 1 \qquad (13)$$

2. Using the calculated $V_{ch}$, find the capacitance $C_{ch}$:

$$C_{ch} \approx \frac{C_{gd}' \cdot (V_{DD} - V_{ch})}{V_{ch}} \qquad (14)$$

3. Find $t_{delay}$: $\quad t_{delay} \approx 5.3 \, R_{GD} \cdot C_{gd}' \qquad (15)$

Find $R_{ch}$:

$$R_{ch} \geq \frac{1}{C_{ch}} \cdot \frac{t_{delay}}{abs \ln \left| 1 - \dfrac{(V_{plt} - V_{ch} - V_{DG})}{V_{DD}} \right|} \qquad (16)$$

**Design Example:**

Given:
$V_{plt}$ = 3.75 V
$Vth_{min}$ = 2 V
$V_{DD}$ = 50 V
$V_{DG}$ = 1 V
$C_{gd}'$ = 0.01 µF
$R_{GD}$ = 1 K.

1. $V_{ch} = 2 - 1 = 1$ V

2. $C_{ch} = \dfrac{0.01\ \mu F\ (50 - 1)}{1} = 0.49\ \mu F$

3. $t_{delay} = 5.3\ (0.01\ \mu F \cdot 1K) = 53\ \mu s$

4. $R_{ch} \geq \dfrac{1}{0.49\ \mu F} \cdot \dfrac{53\ \mu s}{abs\ \ln \left| 1 - \dfrac{(3.75 - 1 - 1)}{50} \right|} \geq 3K$

## CONCLUSION

Active inrush current limiting can be accomplished with a single MOSFET and few external passive components. But in an environment where high dv/dt is observed, the designer must make sure that initially the MOSFET remains off. In order to divert the charge at the gate of the device, a small capacitance $C_{ch}$ can be added. Using the appropriate equations, correct values for $C_{ch}$ and $R_{ch}$ can be obtained which will prevent false turn on due to high dv/dt. In a noisy environment, the charge capacitance will divert much of the noise away from the gate of the MOSFET.

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