SEMICONDUCTOR

AN4507

Gate Drive Considerations For Maximum IGBT Efficiency

Application Note

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This note describes considerations that should be taken into account when designing a gate drive circuit for an IGBT, and gives some typical circuit suggestions.

When designing a gate drive for an application the following items should be considered:-

1) Conduction Losses

2) IGBT Switching Losses

3) Anti Parallel Diode Switching Losses

4) Device Protection

5) Drive Circuit Isolation and Control Signal Transmission

6) Circuit Layout

1.1 CONDUCTION LOSSES

When an IGBT is turned on the collector emitter voltage Vce is a function of gate emitter voltage Vge. As V_{ge} is increased the conduction losses are reduced. It is desirable therefore to increase V_{ge}. to the maximum allowed on the data sheet to minimise the conduction losses, however device manufacturers only guarantee short circuit capability with a Vge of 15V or less. A typical output characteristic for an IGBT is given fig.1.

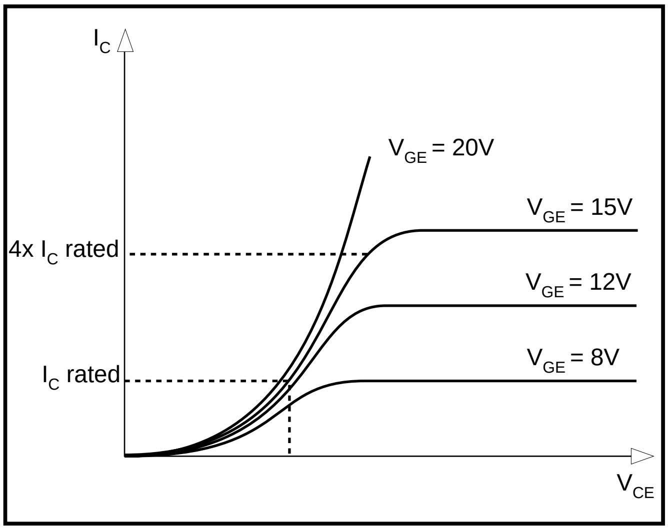

Fig. 1 Typical output characteristics

1.2 IGBT SWITCHING LOSSES

When turning an IGBT on or off the switching losses of the device are affected by the level of Vge and the Gate Resistance (R_g). The effect of increasing V_{ge} or reducing R_g is to reduce the delay time, rise time and fall times of the device and hence to reduce the switching losses. Reducing the level of V_{ge} or increasing R_g results in increased switching losses, but can reduce Electromagnetic Emissions (EMI). Other factors affecting the switching losses are the anti parallel diode (FWD), circuit inductance, snubbers, device junction temperature, operating voltage and current etc.

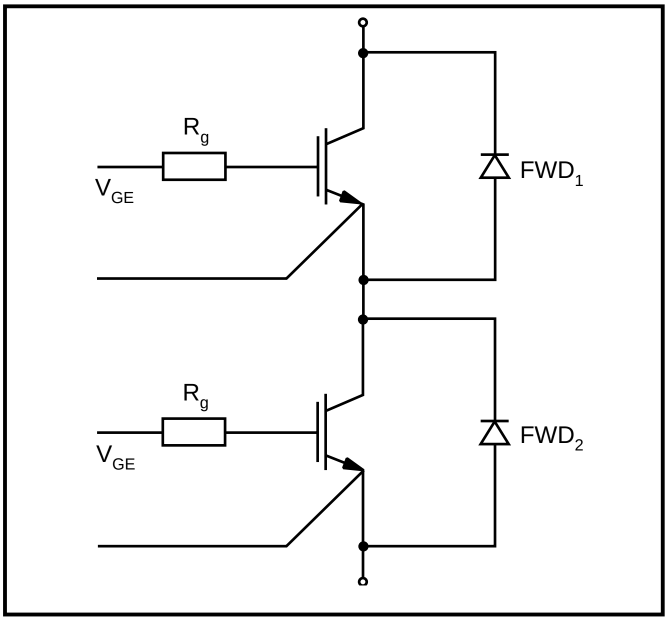

Fig. 2

1.3 ANTI PARALLEL DIODE SWITCHING LOSSES

The reverse recovery and turn on characteristics of the FWD are affected by all the factors mentioned in 1.2, and can therefore be controlled to a certain extent by adjusting the speed of the IGBT. In the event of a diode becoming too snappy in an application, the IGBT turn on can be slowed down, hence reducing the value of di/dt applied to the diode and so reducing the diode losses. However, this is at the expense of increasing the IGBT losses. An alternative method of reducing the FWD losses in a bridge configuration is to turn on the IGBT with a reduced V_{ge}. This limits the peak reverse recovery current, I_{rr}, of the FWD in the opposite side of the arm, according to the IGBTs' forward output characteristic, (see fig.1).

1.4 DEVICE PROTECTION CONSIDERATIONS

The majority of IGBT manufacturers guarantee that IGBTs will withstand a short circuit for 10µs at 50% of the devices rated voltage, with a Vge of 15V and a starting temperature of <125˚C. Two different types of short circuit conditions should be considered.

i) When a device is switched into an already existing short circuit (see fig 3 for typical waveforms).

ii) When a short circuit appears whilst the device is already conducting (see fig 4).

In the second instance both the voltage and collector current rise very quickly. The rapidly rising dv/dt coupled with the miller capacitance can increase the effective Vge seen by the IGBT, further increasing the short circuit current level (see equation [1]). For this reason it is good practice to connect some back-to-back zener diodes directly across the gate emitter terminals to limit the level of V_{ge} (see fig 5).

$$V_{ge} = C \, dv/dt * R_g + V_g \qquad [1]$$

If the device is switched into an already existing short circuit the dv/dt problem does not exist, and the miller effect is not considered to be as significant a problem.

If the value of R_g is increased the rise time of the short circuit current can be increased, reducing the energy loss during the short circuit. At turn off an increased Rg can slow the devices di/dt hence reducing over voltages.

When a device experiences a short circuit, the current is limited according to the devices transfer characteristic. Assuming a Vge of 15V the short circuit current can reach values of 3 to 4 times the devices rated forward current.

The fault current can be reduced by reducing V_{ge}. If the user reduces V_{ge} to <15V, the period of time for which the short circuit can be with stood is increased. This circuit is shown in fig 6.

If a device is being used in a application with a Vge of >15V manufacturers will not guarantee the device will turn of the resulting fault current. The current can increase to levels in excess of 10 times the devices rated current. The user should also be aware that when turning off fault currents the di/dt is considerably greater than is seen under normal operation and the overshoot voltages due to parasitic inductances are increased.

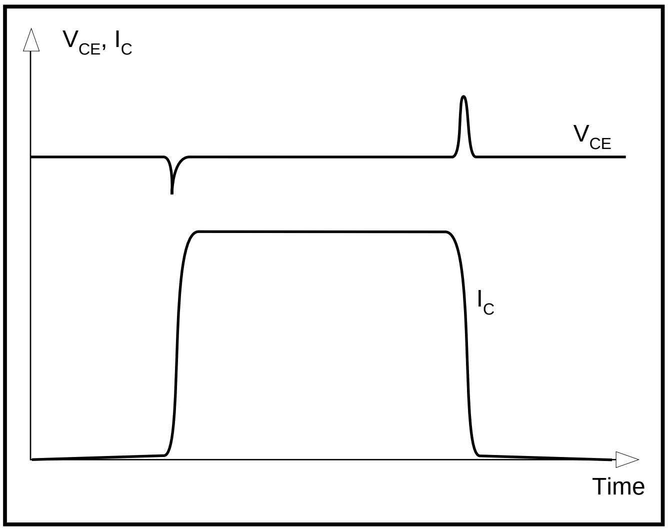

Fig. 3 Typical I_C and V_{CE} waveforms of IGBT being switched into a short circuit

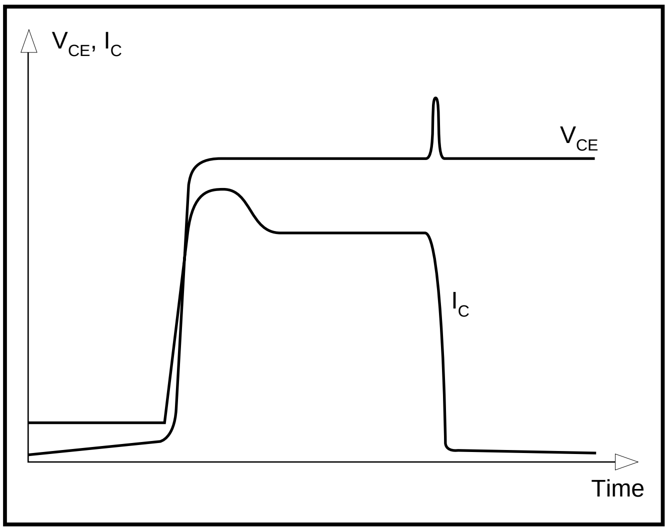

Fig. 4 Typical waveforms of I_C and V_{CE} of IGBT being switched into a short circuit

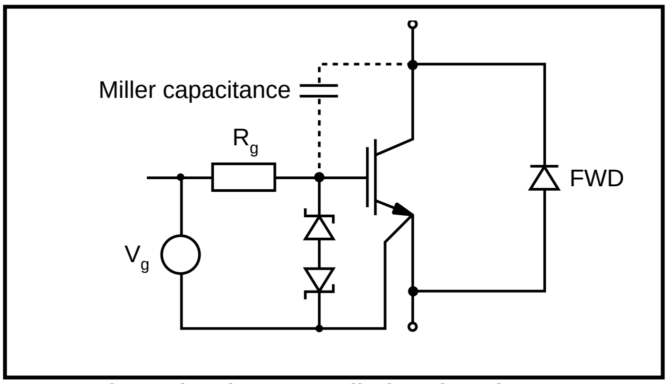

Fig. 5 Showing Zener diodes clamping V_{GE}

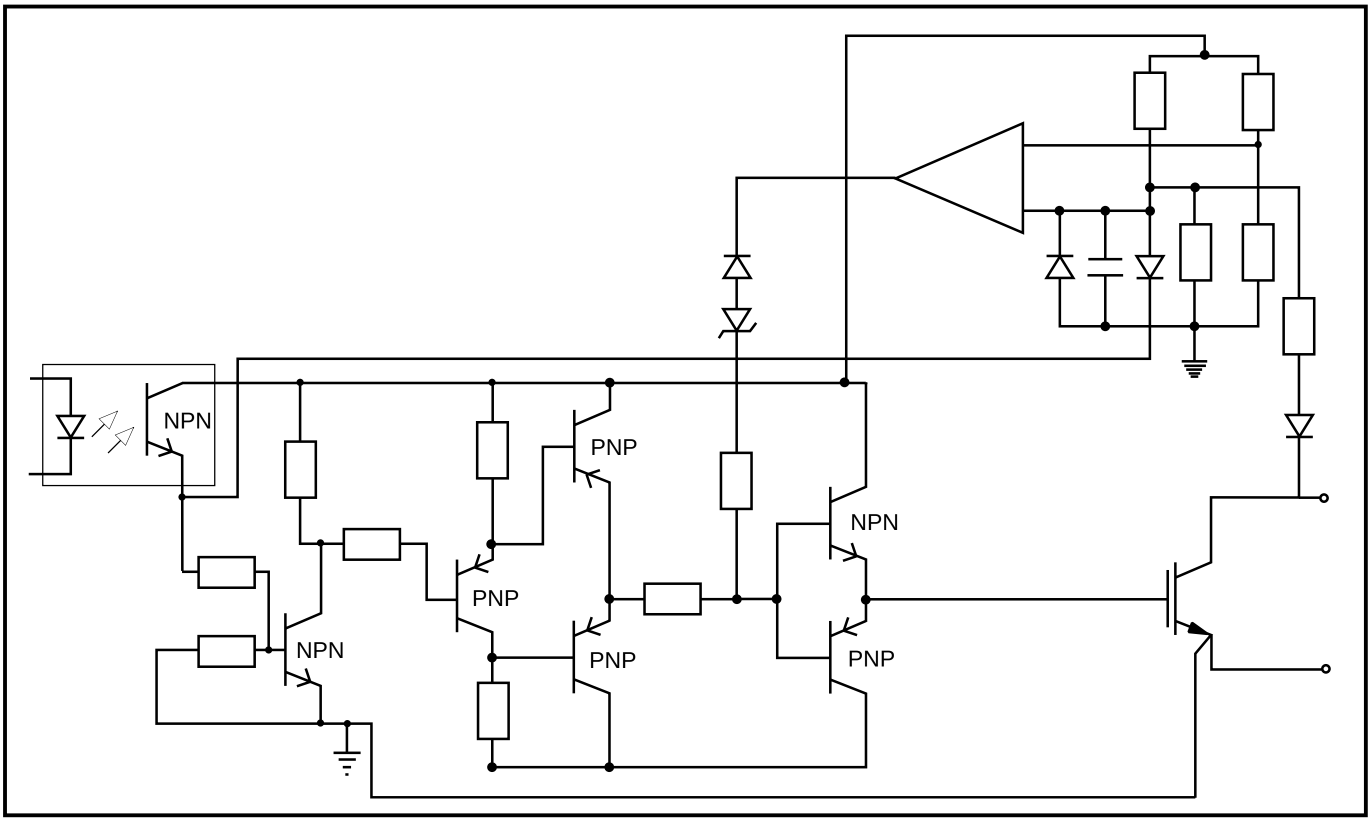

Fig. 6 Schematic showing method of reducing gate drive voltage

1.4-1 THE USE OF NEGATIVE GATE BIAS

In addition to the above considerations it is recommended to use a negative gate bias of -15V when turning off an IGBT during a short circuit. A negative bias of -5V is often recommended as being the minimum negative bias required. A negative bias is essential when turning off a fault current for the following reasons. The threshold voltage Vth reduces by approximately 10mV/C junction temperature rise. Under fault conditions the Vth can be as much as 2V below the 25˚C figure quoted on the data sheet. Also inherent parasitic and mutual inductance within the IGBT module can introduce a further reduction in the turn off voltage seen by the individual IGBT chips in the module, (see fig 7).

The negative bias is also useful for minimising the risk of FWDs snapping off at high dv/dts, causing the IGBT device in parallel with the FWD to turn back on due to the Miller capacitance effect.

1.4-2 GATE DRIVE FAILURE PROBLEMS

Other important issues to consider are failure of the gate drive or the effect due to temporary loss of power. If the gate drive circuit fails it is helpful to have known fail safe condition. This can easily be achieved by introducing a resistor into the gate emitter connection that will discharge the gate emitter in the event of the gate drive losing power, (see fig.8).

The majority of problems with current sharing can be minimised by ensuring that the current paths to the individual modules are the same length and arranging the leads to equalise the effect of any mutual inductances between current paths to the individual paralleled modules.

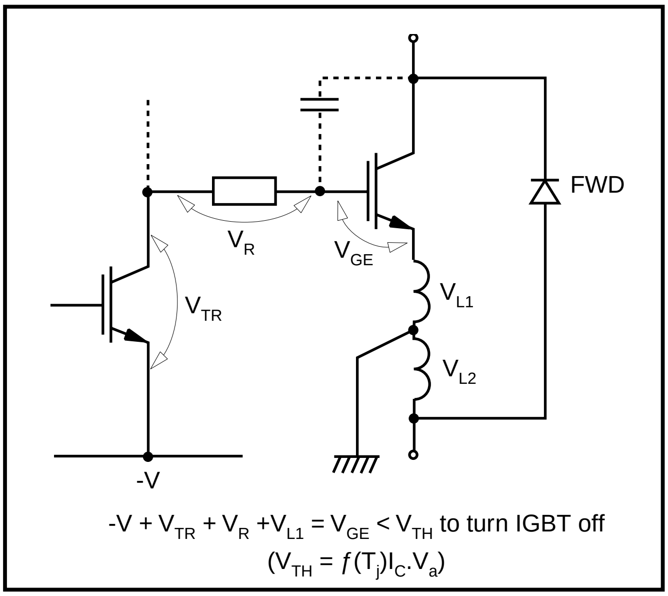

Fig. 7 Circuit showing effect of parasites

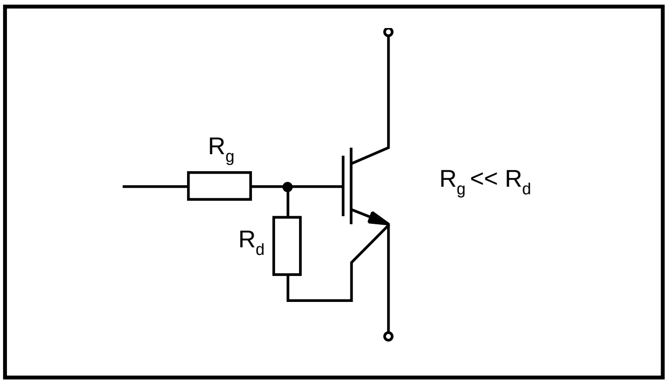

Fig. 8 Circuit showing failsafe resistor

1.5 DRIVE CIRCUIT ISOLATION AND CONTROL SIGNAL TRANSMISSION

In power electronic circuits it is usually necessary to isolate the drive circuit components from the control circuitry. Power is normally transmitted to the drive circuit via a transformer (see fig 9). The control and fault signals can also be transmitted to and from the drive circuit via transformers or alternatively by opto isolators. Whatever method is used, care should be taken to ensure that there is sufficient, voltage capability, speed, and immunity to dv/dt.

1.6 CIRCUIT LAYOUT

Particular attention should be given to the drive circuit layout to maximise noise immunity to parasitic circuit elements, and also to ensure that the correct tracking distances are maintained for the operating voltage being used. If wires have to be used to connect the drive circuit to the gate and emitter connections of the IGBT they should be kept as short as possible. They should also be twisted together to reduce the effect of any noise voltages that may be induced in the wires. It is bad practice to connect the emitter connection of the gate circuit into the path of the collector-emitter current. This is due to the very high load current di/dt's present in the circuit and the inherent parasitic inductance in any conductor. A special case where this may be considered as an advantage is when it is used to improve sharing during the switching operation of parallel devices, by providing negative feedback to the gate voltage, thereby slowing down the switching operation of the faster devices in the network. This is not recommended by Dynex Semiconductor. When considering the transient current sharing of a number of paralleled modules, a slight difference in emitter potentials in the power circuit can give rise to oscillations in the drive circuit.

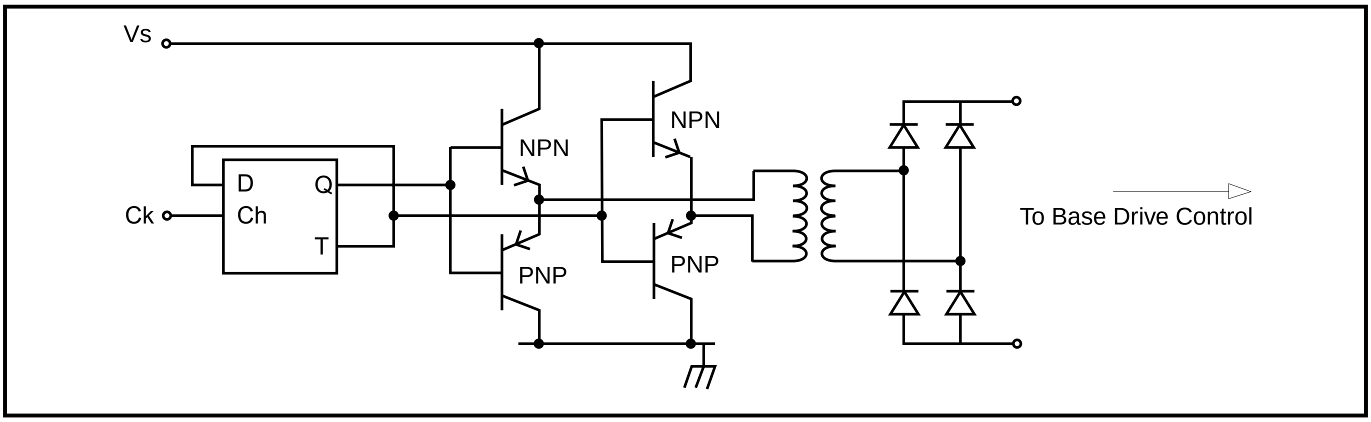

Fig. 9 Circuit showing simple method of supplying power via a transformer

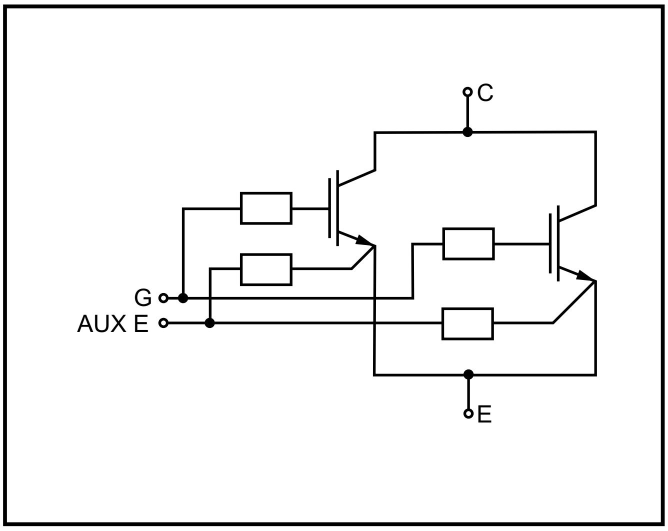

Fig. 10

To damp these oscillations it can be helpful to place the gate resistor in the gate emitter connection to the IGBT rather than in the traditional gate connection (see fig 10).

2.0 DESCRIPTION OF THE GATE DRIVE AND IGBT TURN OFF WAVEFORMS

The turn off behaviour of an IGBT can be split into 4 phases as follows:

1. Gate is discharged until gate emitter voltage reaches the miller plateau and the collector emitter voltage begins to rise slowly.

2. Collector-Emitter voltage rises quickly. The rate of rise of this voltage can be controlled by altering either the gate resistor or the gate turn off voltage. With a large resistor the rate of rise of voltage is very slow. If the gate resistance is reduced until the rate of voltage rise is limited by the rate of current rise then further reductions in Rg have no beneficial effect.

3. When the Collector-Emitter voltage has reached the DC link voltage the current in the IGBT falls rapidly. This rapid current fall causes an over voltage due to parasitic inductance in the circuit. An additional over shoot is caused by the VFR of the FWD diode turning on. The initial rate of fall of current is independent of the gate drive circuit if Vge is below the threshold voltage, but it can be slowed if the gate emitter voltage is slightly above the threshold voltage at turn off. This however causes significant increase in switching losses and should only be used to remove fault conditions

4. The last stage of the turn off process is the decay of the tail current which cannot be controlled by the gate drive.

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