

Abstract

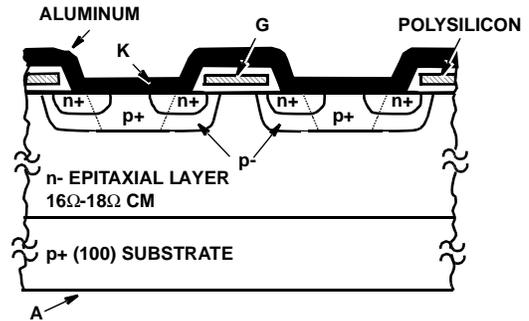
A new MOS gate-controlled power switch with a very low on-resistance is described. The fabrication process is similar to that of an n-channel power MOSFET but employs an n⁻-epitaxial layer grown on a p⁺ substrate. In operation, the epitaxial region is conductivity modulated (by excess holes and electrons) thereby eliminating a major component of the on-resistance. For example, on-resistance values have been reduced by a factor of about 10 compared with those of conventional n-channel power MOSFETs of comparable size and voltage capability.

Introduction

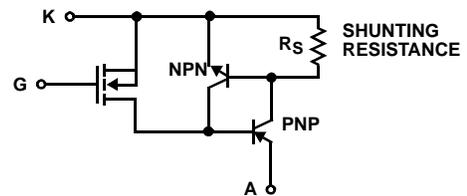
Vertical MOSFETs have become increasingly important in discrete power device applications due primarily to their high input impedance, rapid switching times, and low on-resistance. However, the on-resistance of such devices increases with increasing drain-source voltage capability,^[1-3] thereby limiting the practical value of power MOSFETs to applications below a few hundred volts. In this letter, we describe the fabrication and characteristics of a new vertical power MOSFET structure that provides an on-resistance value about 10 times smaller than that of conventional power MOSFETs of the same size and voltage capability. In this device, the conductivity of the epitaxial drain region of a conventional MOSFET is dramatically increased (modulated) by injected carriers; this mechanism results in a significant reduction in the device on-resistance and leads to the acronym IGBTs (Insulated Gate Bipolar Transistor).

This device, while similar in structure to the MOS-gated thyristor,^[4,5] is different in a fundamental way; it maintains gate control (doesn't latch) over a wide range of anode current and voltage.^[6] The structure and the equivalent circuit for the IGBTs are shown in Figure 1(a) and (b); they are similar to those of an MOS-gated thyristor, except for the presence of the shunting resistance R_S in each unit cell. The fabrication is like that of a standard n-channel power MOSFET except that the n⁻-epitaxial Si layer is grown on a p⁺ substrate instead of an n⁺ substrate. The heavily doped p⁺ region in the center of each unit cell, combined with the sintered aluminum contact shorting the n⁺ and p⁺ regions, provides the shunting resistance shown in Figure 1(b). This has the effect of lowering the current gain of the n-p-n transistor (α_{n-p-n}) so that α_{n-p-n} + α_{p-n-p} < 1. Thus latching is prevented and gate control is maintained within a large operating range of anode voltage and current.^[6]

REGION	THICKNESS (μm)
EPI	60 - 62
n ⁺	1.0 - 1.5
p ⁻	3.5 - 4.0
p ⁺	5.0 - 5.5



(A) STRUCTURE



(B) EQUIVALENT CIRCUIT

In the remainder of this note we describe the operation and characteristics of this device.

Device Operation

The IGBT is a four-layer (n-p-n-p) device with an MOS-gated channel connecting the two n-type regions. In the normal mode of operation, a positive voltage is applied to the anode (A) relative to the cathode (K). When the gate (G) is at zero potential with respect to K, no anode current (i_A) flows for anode voltage V_A below the breakdown level V_{BF}. When V_A < V_{BF} and the gate voltage is larger than the threshold value V_{GT}, electrons pass into the n⁻-region (base of the p-n-p transistor). These electrons lower the potential of the n⁻-region, forward biasing the p⁺ - n⁻ (substrate-epi-layer) junction, thereby causing holes to be injected from the p⁺ substrate into the n⁻ epi-layer region. The excess electrons and holes modulate the conductivity of the high-resistivity n-region, which dramatically reduces the on-resistance of the device. During normal operation, the shunting resistor (R_S) keeps the emitter current of the n-p-n transistor very low, which keeps α_{n-p-n} very low. However, for sufficiently large i_A, significant emitter injection may occur in the n-p-n transistor, causing α_{n-p-n} to increase; in this case the four-layer device may latch, accompanied by loss of control by the MOS gate. In this event, the device may be turned off by lowering i_A below some "holding" value, as is typical of a thyristor.

Device Characterization

Two different lots of IGBT structures, consisting of about 10 wafers/lot, have been successfully prepared to date. From these wafers, 1.5mm and 3mm square devices were fabricated using a standard HEXFET geometry^[7] with a polysilicon gate electrode over an SiO₂ gate dielectric.

Several hundred IGBT were mounted in standard TO-3 and TO-66 packages and characterized under DC and pulsed conditions, as described below.

With zero gate bias, the forward characteristic of a IGBTs shows very low current (<1nA) up to about 390V, where it breaks up sharply to much larger current levels with only a slight increase in voltage. If the internal junction between the p⁺ substrate and the n⁻ epitaxial layer had been edge-passivated, a similar reverse breakdown characteristic would be expected. The actual reverse breakdown voltage for our devices was about 100V because edge passivation was not used.

Figure 2(a) shows the MOSFET-like transfer characteristics of an IGBT in the low gate-voltage region. A noteworthy feature of the IGBT characteristic is the ~0.7V offset, from the origin, of the steeply rising portion of the i(v) characteristics. This offset is the voltage required to forward bias the p⁺ - n⁻ (substrate-epi-layer) junction, and is an integral characteristic of the present device.

Figure 2(b) shows the i(v) characteristic of an IGBT with V_G = 20V, and demonstrates the low on-resistance of the device (~0.084Ω at 20A). The on-resistance values of nearly all of the many IGBT fabricated to date have been less than 0.1Ω (at 20A) for the 3mm square devices. Such values compare very favorably with those of conventional power MOS structures, as illustrated in Figure 3. Here, the open data points (and the upper curve) are from data sheet specifications of commercial power MOSFETs (Fairchild, IRC, and Motorola). The solid data points (and the lower curve) are those of Baliga, which he labelled "state-of-the-art",^[3] supplemented with some of the "best" of Fairchild' commercial and developmental MOSFETs. Note that the on-resistance of the IGBT is approximately 10 times less than that of a 400V state-of-the-art MOSFET. Moreover, similarly low on-resistance values should be obtainable from IGBT designed for higher drain-source voltages. This is due to the fact that the resistance of the modulated region is determined by the concentrations and mobilities of the excess carriers (as in a p-i-n diode)^[8] rather than by the background doping of the layer. In particular, the epi-layer doping and thickness of our present IGBT structures were designed for 600V, but V_{BF} was limited to 400V by the edge design of the device. An improved edge design should provide a blocking capability closer to bulk breakdown, without altering the on-resistance of the device. This would make the IGBTs on-resistance of less than 0.1Ω even more attractive for high-voltage applications.

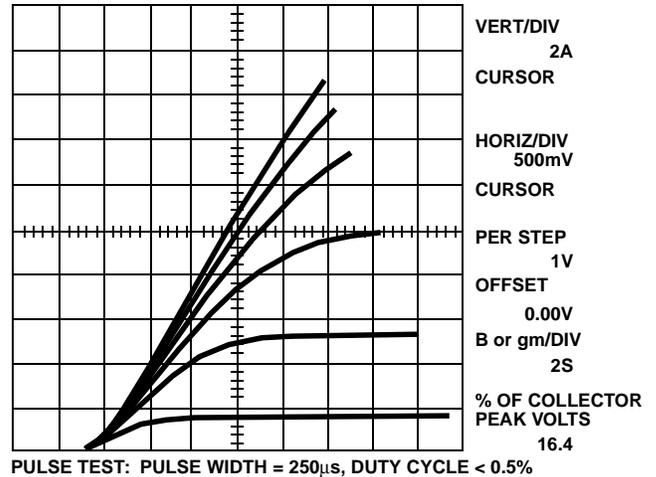


FIGURE 2A MOSFET - LIKE CHARACTERISTIC

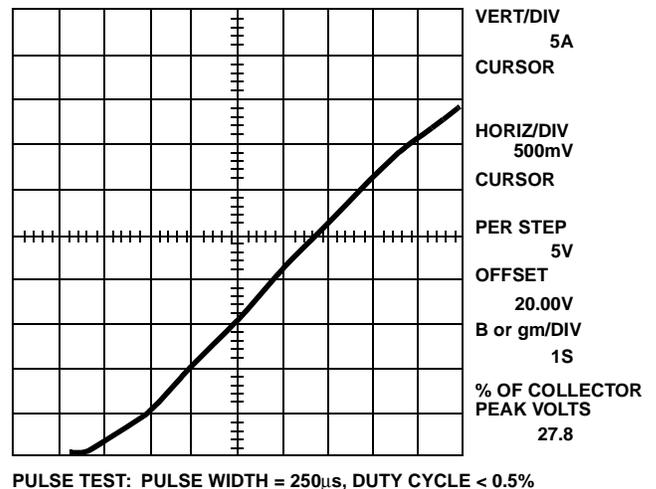


FIGURE 2B. IGBT i(v) with V_G = 20V

Transient Response Measurement

Switching time measurements under pulsed gate-voltage operation were used to characterize the transient operation of the device. The response of the anode current to a square-wave gate-voltage pulse is comprised of a rapid turn-on (with a typical time less than 1μs) and a somewhat slower turn-off. We observed that the turn-off transient consists of an initial "fast" component, followed by a "slow" tail, as shown in Figure 4.

We believe that the initial rapid decay is due to the turn-off of the MOS portion of the equivalent circuit, and the turn-off tail is due to the time required for the excess carriers in the epitaxial drain region to decay. In general, turn-off times in the range of 5μs to 20μs were observed, with the precise value depending on circuit conditions and the turn-off time of the gate pulse.

The n-p-n-p structure of the IGBTs is similar to that of a thyristor and can be forced to latch under sufficiently high drive conditions. We have observed latching currents in the range 10A - 30A in 3mm square chips. The magnitude of the latch-

ing current has been found to depend on both anode voltage and temperature, decreasing with increasing anode voltage or increasing temperature.

More interestingly, the latching current is also strongly influenced by the gate voltage turn-off time. Slow gate turn-off (~10μs) permits anode currents up to 30A without latching. However, rapid gate turn-off (≤ 1μs) leads to latching at a much lower anode current level (~10A) in the same device. We believe that latching during rapid turn-off of the gate voltage is due to current being forced through the n-p-n transistor causing αn-p-n to increase, and leading to the condition for latching, αn-p-n + αp-n-p = 1. Slow turn-off of the gate voltage prevents this, since the induced channel turns off slowly and partially shunts the n-p-n transistor; the small current through this transistor keeps αn-p-n sufficiently low to avoid latching.

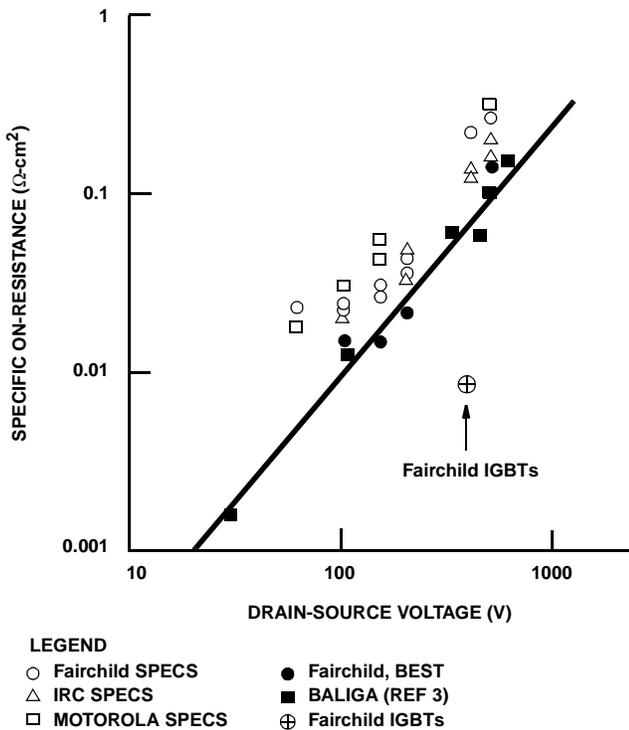


FIGURE 3. SPECIFIC ON-RESISTANCE vs DRAIN-SOURCE VOLTAGE CAPABILITY FOR STATE-OF-THE-ART POWER MOSFETS AND THE IGBTs

Summary

A new MOS-gate-controlled power device, the IGBTs, has been described. The device has the desirable feature of a very low on-resistance similar to that of a thyristor, but is capable of maintaining gate control of the anode current over a wide range of operating conditions. The low on-resistance is due to conductivity modulation of the n epitaxial layer equivalent to the extended drain in a power MOSFET; this carries with it the penalty of slow switching compared with that of a conventional power MOSFET.

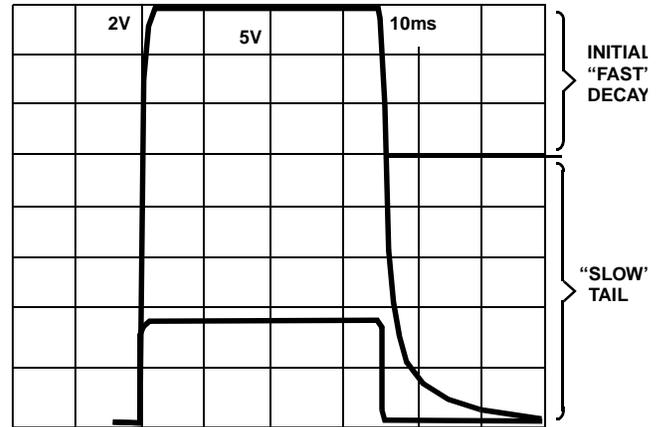


FIGURE 4. GATE VOLTAGE (LOWER TRACE) AND ANODE CURRENT (UPPER TRACE) WAVEFORMS FOR $i_A(\text{MAX}) = 8\text{A}$

Acknowledgment

The authors gratefully acknowledge the various helpful contributions of C. Nuese, D. Bergman, R. Ford, R. Jarl, G. Looney, P. Robinson, W. Romito, L. Skurkey, R. Stolzenberger, C. Wheatley, J. Wojslawowicz, and the staff of the Integrated Circuit Technology Center at RCA Laboratories. Added Note: Following submission of this Note, a similar device was described by B. J. Baliga in a presentation on December 14, 1982 at the International Electron Devices Meeting in San Francisco, CA. (B. J. Baliga et al., "The Insulated Gate Rectifier (IGR): A New Power-Switching Device", in IEDM Tech. Dig. 1982, pp 264-267.

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