Application Note

AN2409/D
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Small Outline Integrated Circuit--Fine Pitch Package (SOIC)

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CONTENTS

1.0 PURPOSE

This Application Note provides general package information including package dimensions, guidelines for printed circuit board (PCB) layout, package and board level reliability, electrical parasitics, and thermal resistance.

2.0 SCOPE

This Application Note is specific to the fine pitch Small Outline Integrated Circuit Package (SOIC). For the SOIC package, fine pitch is defined as lead pitch of 0.65mm and smaller. Information on 32 and 54 leaded SOICW packages are presented in this document. This document serves only as a guideline to help develop user specific solution. Actual experience and development efforts are still required to optimize the process per individual device requirements and practices.

3.0 SOIC PACKAGE

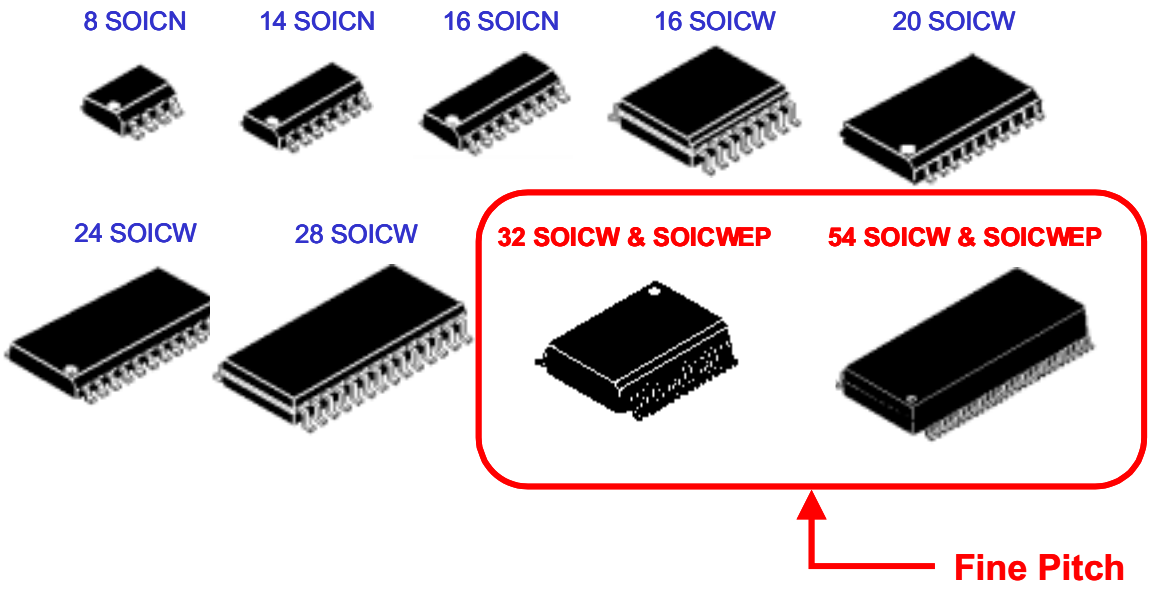


Figure 1. SOIC Package Family

Figure 1 shows the different SOIC packages offered through Motorola. The packages highlighted in red border and fonts are the ones covered in this document. Both the non-exposed and exposed pad (denoted as '–EP') versions of the fine pitch SOICW packages are discussed.

3.1 Package Description

A SOIC is a leaded surface mount package with "gull wing" lead form, where the leads are bent outwards at the tip. This bent lead tip area is the seating plane and the area bonded to the PCB.

SOIC packages are available in narrow (denoted as SOICN), standard (SOIC), and wide (SOICW) package body width sizes (See Figure 1). At the time of this Application Note, all the fine pitch SOIC packages were only available in the wide package body widths. The SOIC package is also available in non-exposed pad and exposed pad (denoted as '-EP') versions. The exposed pad package has the center leadframe area exposed to the bottom side of the package, mainly for thermal performance improvement (See Figure 2 and Figure 5). This exposed pad region is soldered to the PCB and the majority of the heat is dissipated through this region. The non-exposed pad version has the mold compound covering the entire bottom side of the package. There is another method of enhancing the thermal performance of the SOICW package, it is called the fused leadframe SOIC package. The fused leadframe SOICW package connects a few of the internal leads to the die attach region to dissipate some of the heat. The fused leadframe design is internal to the molded area and it cannot be detected from the outside of the package.

Table 1. SOIC Package Acronyms

Package Acronyms	Package Description	Body Width Min & Max (mm)
SOIC	Standard SOIC non-Exposed Pad	5.10—5.45mm
SOICN	SOIC Narrow Body non-Exposed Pad	3.80—4.00mm
SOICW	SOIC Wide Body non-Exposed Pad	7.40—7.60mm
SOICW-EP	SOIC Wide Body Exposed Pad	7.40—7.60mm

The fine pitch SOICW packages are available in both Cu leadframes post plated with SnPb and with NiPdAu preplated leadframes. The NiPdAu preplated leadframe is the Pb-free solution for this package.

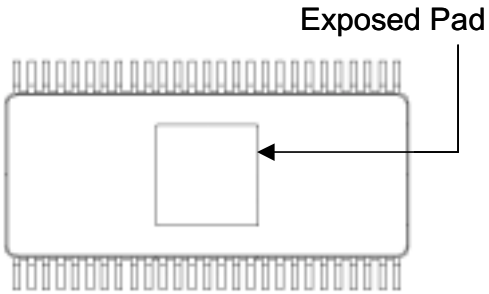


Figure 2. 54ld SOIC-EP Backside View

3.2 Package Dimension

The non-exposed pad and exposed pad versions have the same package body widths, and lead configurations. The difference is in the body length and for the exposed pad version, the exposed pad dimensions offered.

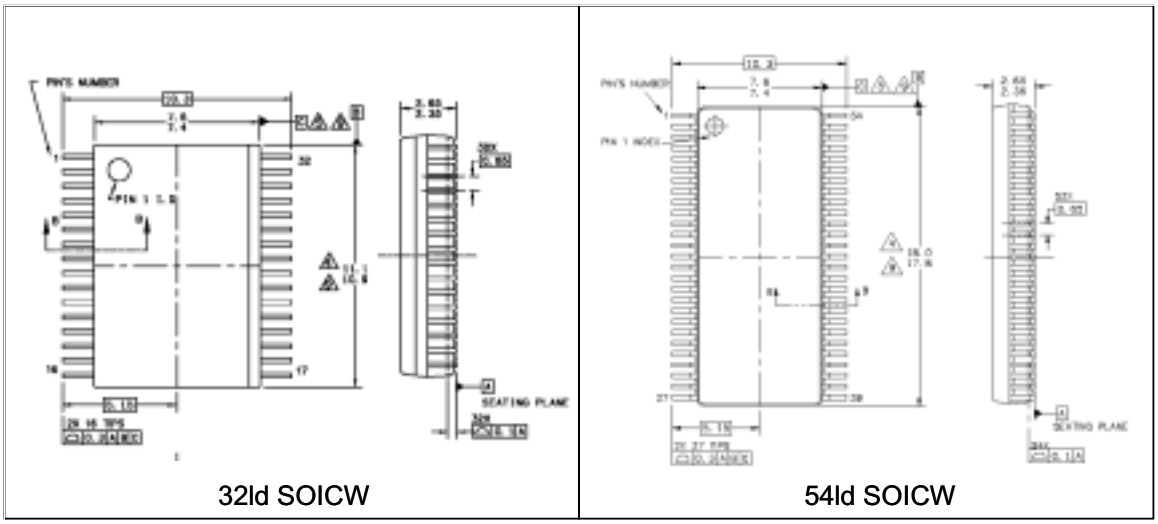


Figure 3. Top and Side Views of the 32ld and 54ld SOICW Packages

Table 2. Package Dimensions

Dimensions	32ld (Min - Max in mm)	54ld (Min - Max in mm)
Package Length	10.90—11.10	17.80—18.00
Package Width (with Leads)	10.00—10.60	10.00—10.60
Package Body Width	7.40—7.60	7.40—7.60
Package Height	2.35—2.65	2.35—2.65

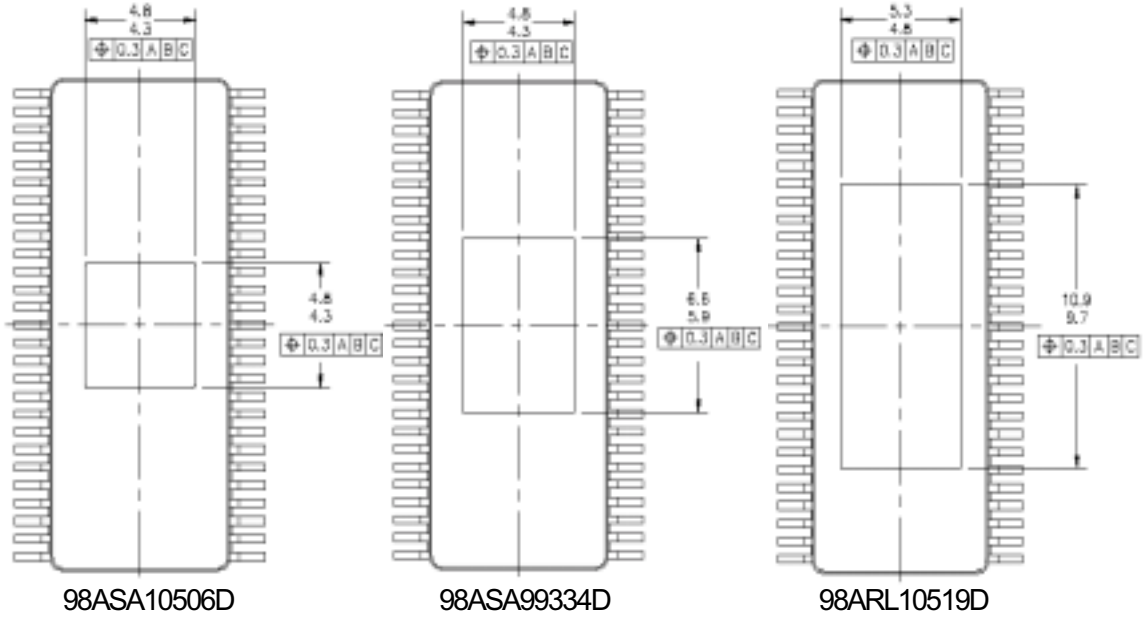


Figure 4. Three Different 54ld SOICW-EP Packages. Backside View Only

The various 54ld SOICW-EP packages available are shown in Figure 4. The dimensions are provided, below, in Table 3

Table 3. 54ld SOICW-EP Packages

Package Dimension	98ASA10506D*	98ASA99334D*	98ARL10519D*
Exposed Pad Y Dim.	4.55mm	6.25mm	10.30mm
Exposed Pad X Dim.	4.55mm	4.55mm	5.05mm
*Note: Nominal dimensions shown. The '98AXXXXXXXD' number represents the Motorola Case Outline Drawing number.			

3.3 Package Cross Section

The cross section drawings in Figure 5 was included to show the internal leadframe design differences between the non-exposed SOICW package and the exposed pad SOICW-EP package.

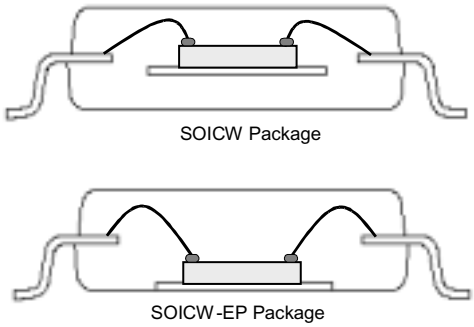


Figure 5. Cross section SOICW Package (Top) & SOICW-EP Package (Bottom)

3.4 Process Flow

The assembly process flow is dependent upon the factory site, but the general process flow is presented, below, in Figure 6.

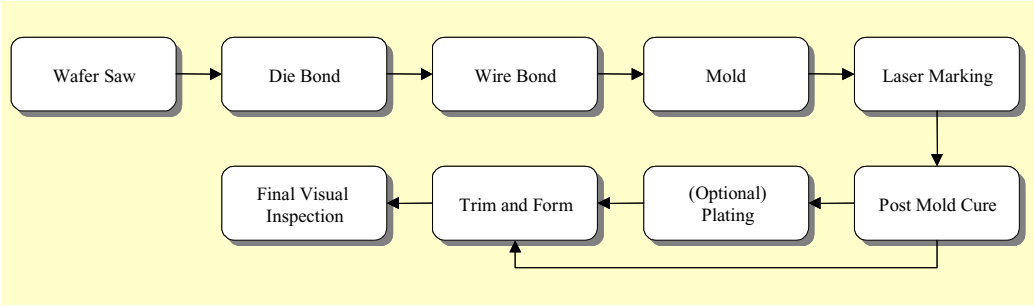
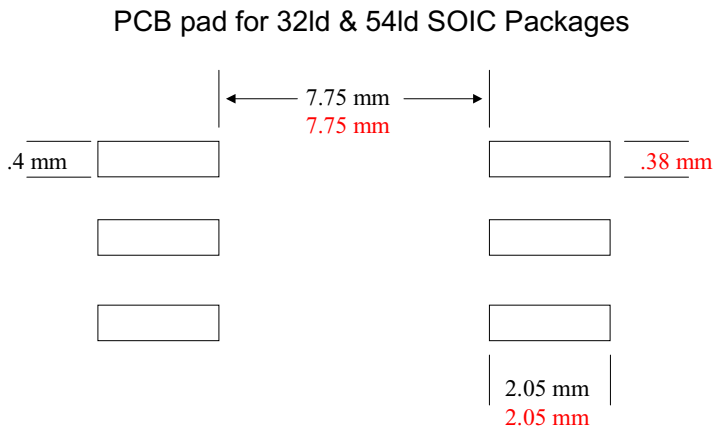


Figure 6. General SOICW Process Flow

4.0 PRINTED CIRCUIT BOARD (PCB) LEVEL GUIDELINES

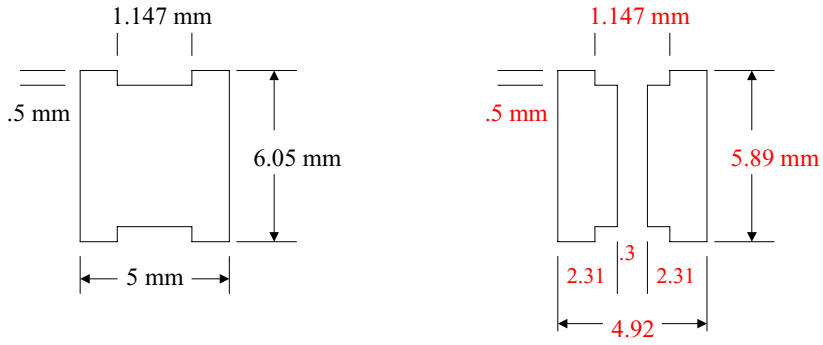
4.1 PCB Design Guideline

The PCB pad and stencil aperture dimensions in Figure 7, Figure 8, Figure 9, Figure 10, and Figure 11 are recommended for the 32ld and 54ld SOICW packages [11]. This is based on package dimensions presented in Section 3.2 Package Dimension. Note Figure 9, Figure 10, and Figure 11 relate to the 54ld SOICW-EP packages with the exposed pad dimensions provided in Table 3. Dimensions in red font represent the solder stencil aperture dimensions, and the dimensions in black font represent the PCB pad dimensions. As stated earlier under Scope, dimensions are provided as guidelines. The stencil and PCB pad dimensions may vary dependent upon application.



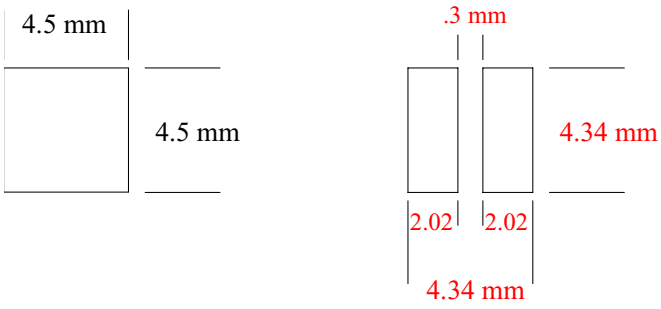
PCB dimensions shown in black.
Solder paste stencil apertures shown in red.

Figure 7. PCB Pad Dimensions for Lead of 32ld and 54ld SOICW & SOICW Packages



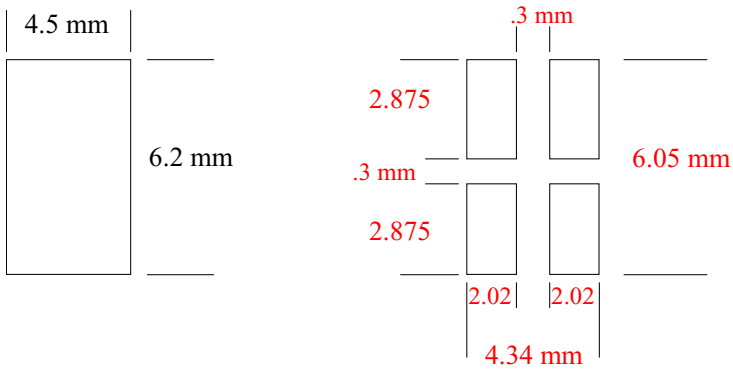
PCB dimensions shown in black.
Solder paste stencil apertures shown in red.

Figure 8. PCB Exposed Pad Dimensions for 32ld SOICW-EP Package



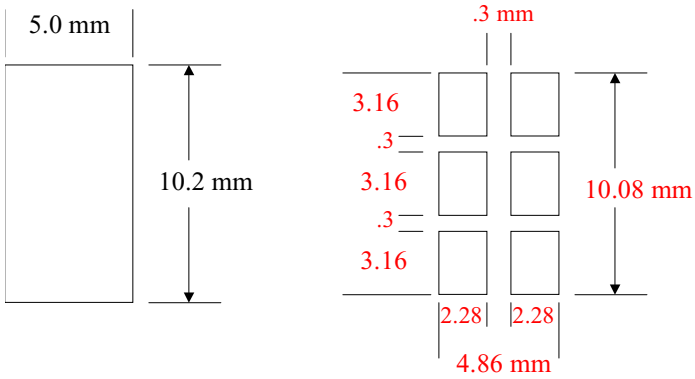
PCB dimensions shown in black.
Solder paste stencil apertures shown in red.

Figure 9. PCB Exposed Pad Dimension for 54ld SOICW-EP Package (98ASA10506D)



PCB dimensions shown in black.
Solder paste stencil apertures shown in red.

Figure 10. PCB Exposed Pad Dimensions for 54ld SOICW-EP Package (98ASA99334D)



PCB dimensions shown in black.
Solder paste stencil apertures shown in red.

Figure 11. PCB Exposed Pad Dimensions for 54ld SOICW-EP Package (98ARL10519D)

5.0 1ST LEVEL RELIABILITY

The Moisture Sensitivity Level (MSL) rating for 32ld SOICW package is MSL2/3 @ 240°C. The MSL rating for 54ld SOICW package is MSL3 @ 240°C. Both 32ld and 54ld SOICW packages were internally qualified using JEDEC standard, JEDEC-STD-020. Qualification level above MSL 2 or 3@ 240°C will be considered on a case-by-case basis.

6.0 2ND LEVEL RELIABILITY

The 2nd level reliability is board level reliability expressed in terms of solder joint life. In almost all cases, customers are interested in the Time to First Failure (TFF) and Mean

Time to Failure (MTTF) values. The SOIC package, like all leaded package, has a high 2nd level reliability. Unfortunately, actual data for the 32ld and 54ld SOICW packages are not available at this time. The 2nd level reliability model is expected to complete in the first quarter of year 2003. Actual data is only available in the 14ld SOIC package with NiPdAu leadframe. The TFF on the 14ld SOIC was 8815 cycles at –40 to 125°C temperature cycle range. The test ended at 16430 cycles where 79.3% of the units under test failed. At the 0 to 100°C temperature cycle range, the test was stopped when there were no failures at 22738 cycles.

7.0 PACKAGE THERMAL RESISTANCES

The thermal performance of the SOICW package is characterized using two thermal board types and three boundary conditions. Junction-to-ambient thermal resistance (Theta-JA or $R_{\theta JA}$ per JEDEC JESD51-5 [1]) is a one-dimensional value that measures the conduction of heat from the junction (hottest temperature on die) to the environment near the package. The heat that is generated on the die surface reaches the immediate environment along two paths: (1) convection and radiation off the exposed surface of the package and (2) conduction into and through the test board followed by convection and radiation off the exposed board surfaces. The $R_{\theta JMA}$ is similar to $R_{\theta JA}$, but it measures the thermal performance of the package on a board with two signal layers and two internal planes (2s2p). The 2s2p test board is designed per JEDEC JESD51-5 [1] and JEDEC JESD51-7 [2]. $R_{\theta JMA}$ helps bound the thermal performance of the SOICW package in a customer's application. $R_{\theta JMA}$ provides the thermal performance of the SOICW when there are no nearby components dissipating significant amounts of heat on a multi-layer board. Junction-to-board thermal resistance (Theta-JB or $R_{\theta JB}$ per JEDEC EIA/JESD51-8 [3]) measures the horizontal spreading of heat between the junction and the board. The board temperature is taken near the board surface on one of the package center leads. Another thermal resistance that is provided is junction-to-case thermal resistance (Theta-JC or $R_{\theta JC}$). The case is defined as either the temperature at the top of the package, Theta-JC^1 or $R_{\theta JC}{}^1$, and the temperature at the bottom of the exposed pad surface, Theta-JC^2 or $R_{\theta JC}{}^2$. $R_{\theta JC}{}^1$ can be used to estimate the thermal performance of the SOICW-EP package when the board is adhered to a metal housing or heat sink and a complete thermal analysis is done. These thermal resistances help bound the thermal performance under distinct environments.

The different lead count and package versions (non-exposed pad/exposed pad and fused leadframes), board types, and die sizes were identified and modeled under JEDEC conditions listed, above. The results are depicted in Table 4.

Table 4. Thermal Resistance Data

Grp	Package type	EP	LF Config	LF p/n	Flag Size	Die Size
A	32ld SOICW [4]	no	regular	17ARH99135A603	6.66 x 5.55	4.90 X 4.53
B	32ld SOICW [5]	no	4 fused	17ARH99135A604[1]	6.66 x 5.55	4.90 X 4.53
C	32ld SOICW-EP [6]	yes	regular	17ARH99135A605	6.66 x 5.55	4.90 X 4.53
D	54ld SOICW-EP [7][8][9]	yes	regular	17ARL10113D603	6.90 x 5.10	4.90 x 4.53
E	54ld SOICW [7][8][9]	no	regular	17ARL10113D600	6.90 x 5.10	4.90 x 4.53
F	54ld SOICW [7][8][9]	no	regular	17ARL10113D600	6.90 x 5.10	5.90 x 4.20
G	54ld SOICW [7][8][9]	no	12 fused	17ARL10113D601[2]	6.90 x 5.10	5.90 x 4.20
H	54ld SOICW-EP [7][8][9]	yes	regular	17ARL10113D603	6.90 x 5.10	5.90 x 4.20
I	54ld SOICW-EP [7][8][9]	yes	regular	17ARL10113D606	11.15 x 5.55	10.39 X 5.03

			No Wind						
Grp	Package type	EP	Theta JA		Theta JC[1]	Theta JC[2]	Theta JB	Theta JB	
			1S	2S2P	1S	1S	2S2P	2S2P	Board Type
A	32ld SOICW [4]	no	70.0	47.0	21.0	N/A	19.0	N/A	
B	32ld SOICW [5]	no	68.0	45.0	20.0	N/A	15.0	8	
C	32ld SOICW-EP [6]	yes	74.0	27.0	33.0	0.9	8.0	N/A	
D	54ld SOICW-EP [7][8][9]	yes	62.9	24.8	28.4	1.6	8.3	N/A	
E	54ld SOICW [7][8][9]	no	58.7	40.2	17.6	N/A	23.2	N/A	
F	54ld SOICW [7][8][9]	no	58.2	39.7	17.0	N/A	23.2	N/A	
G	54ld SOICW [7][8][9]	no	52.6	33.8	15.6	N/A	16.5	9.3	
H	54ld SOICW-EP [7][8][9]	yes	62.2	24.6	27.8	1.4	8.3	N/A	
I	54ld SOICW-EP [7][8][9]	yes	53.6	21.2	19.8	0.7	6.0	N/A	
			°C/W						
	Notes			1,2	5	4	3	6	

- **17ARH99135A604[1]: 17ARH99135A604 has only 2 fused leads (on one side) to the flag. Model includes 4 fused leads (2 on each side)**
- **17ARL10113D601[2]: 17ARL10113D601 has 12 fused leads. 3 fused leads at each corner of the flag**

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-6 with the board horizontal. 2s2p board is designed per JEDEC EIA/JESD51-5 and JEDEC JESD51-7.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the foot of the center lead. For fused lead package, the adjacent lead is used. 2s2p board is designed per JEDEC JESD51-5 and JEDEC JESD51-7.
4. For exposed pad packages where the pad would be expected to be soldered, junction to case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.
5. According to the mil standard specification, it indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature. Data was bsed on both 1S and 2S2P boards.
6. Theta JB^{6}: junction-to-fused lead. Lead temperature is measured on top surface of the foot of the fused lead (either center fused lead or corner fused lead depending on the fused lead design.

8.0 ELECTRICAL PERFORMANCE

For a leaded package, the series inductance and capacitance contributed by the SOICW leads are higher than those of the leadless package such as the QFN, but in general lower than those of the BGA packages (due to the parasitic effects contributed by the substrate traces). It is important to note, however, that the RLC (RLC stands for resistance, inductance and capacitance) performance comprises contributions of both the terminal and bonding wire. In cases of small die to flag size ratio, longer bonding wires may be required for the same device in the BGA package. In these cases, the RLC performance may be poorer.

A field solver was used to simulate the RLC performance of the 32ld and 54ld SOICW and SOICW-EP packages. The results were graphed and provided in Figure 12 and Figure 13.

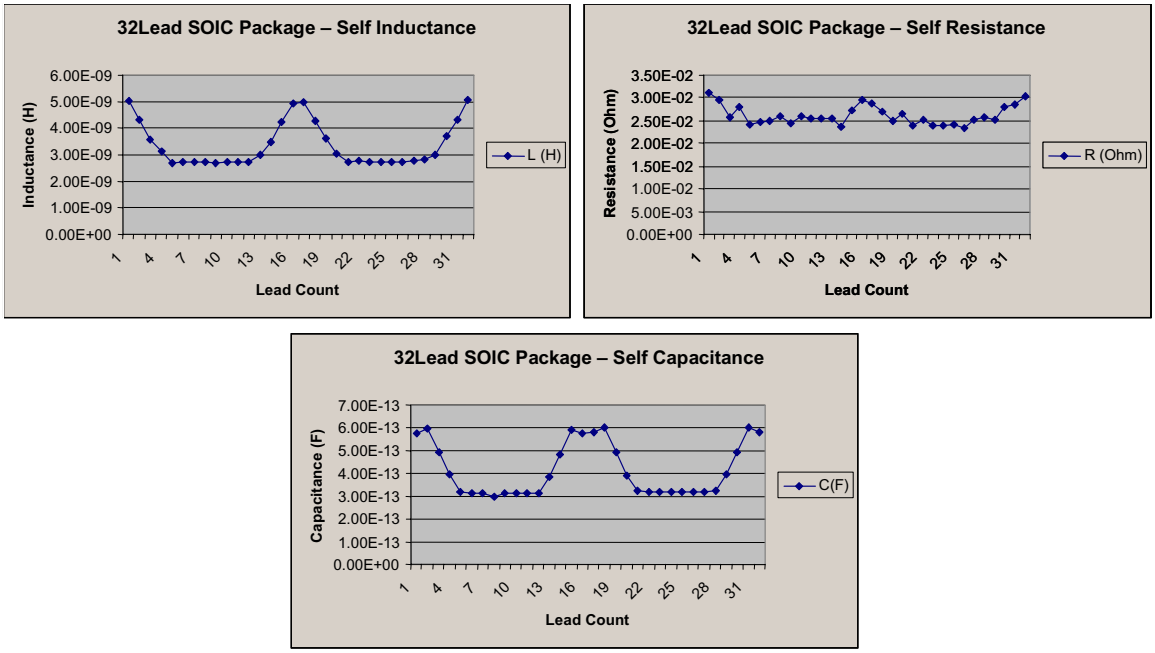


Figure 12. 32ld SOICW and SOICW-EP Electrical Parasitics

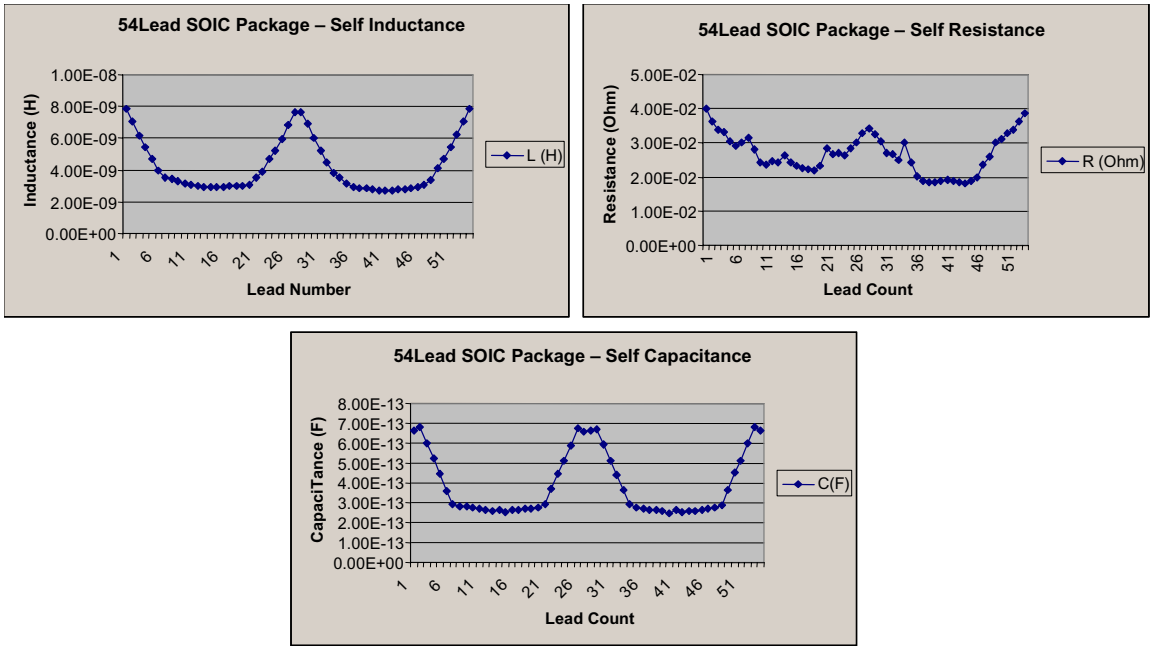


Figure 13. 54ld SOICW and SOICW-EP Electrical Parasitics

9.0 REFERENCE

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[2] EIA/JESD51-7, “High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages,” February 1999.

[3] EIA/JESD51-8, “Integrated Circuit Thermal Test Method Environmental Conditions – Junction-to-Board”, October 1999.

[4] Montes De Oca, Tony, “32ld SOICW Thermal Simulation Report”, Motorola Internal Report, Nov. 21, 2002.

[5] Montes De Oca, Tony, “32ld SOICW Fused Leadframe Thermal Simulation Report”, Motorola Internal Report, April 25, 2002.

[6] Montes De Oca, Tony, “32ld SOICW-EP Thermal Simulation Report”, Motorola Internal Report, May 28, 2002.

[7] Lee, Tom, “Thermal Modeling of an Exposed Pad 54ld SOIC”, Motorola Internal Report, Sept. 7, 2001.

[8] Lee, Tom, Chiriac, Victor, “Thermal Assessment of 54-Lead SOIC Package for SmartMOS Applications”, Motorola Internal Report, April 18, 2001.

[9] Lee, Tom, “Thermal Request FP SOIC Spreadsheet”, Motorola Internal Report, Nov. 2002.

[10] Zhou, Yaping, “32ld and 54ld SOIC Electrical Parasitic Extraction Report”, Motorola Internal Report, Nov 14, 2002.

[11] Burnette, Terry, “PCB Pad for 32ld & 54ld Exposed Pad SOIC Leads”, Motorola Internal Report, Dec 3, 2002.

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