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Application Considerations Using Insulated Gate Bipolar Transistors (IGBTs)

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DEVICE CHARACTERISTICS

The recently introduced Insulated Gate Bipolar Transistor (IGBT) has been undergoing considerable improvement and maturation due to improvement in process technology. This device has become the most popular new device used by the power electronics design engineers. It is quickly replacing most of the power BJTs because of its speed and ease of gate drive. In this section, a brief overview of the device and its characteristics will be presented.

INTRODUCTION

In the power electronics arena there is a constant demand for compact, lightweight, and efficient power supplies. However, the demands for the power converters are not fully satisfied by power bipolar transistors (BJTs) and power MOSFETs. High current and high voltage BJTs are available, but their switching speeds are not satisfactory. Power MOSFETs have high speed switching, but high voltage and high current modules are not available.

The Insulated Gate Bipolar Transistor (IGBT) device is a power semiconductor device introduced to overcome the limitations of the power BJTs and power MOSFETs. This device eliminates the high on–state losses of the MOSFET while maintaining the simple gate drive requirements of that device. This device is controlled by the gate voltage as is the power MOSFET, but the output current is that of a bipolar transistor. These devices combine the best features of both the bipolar transistors and of the MOSFET.

In order to optimally implement all of the advantages of the IGBT device, it is essential that the designer understand the general operating characteristics of the device.

DEVICE STRUCTURE

A schematic structure of an N–channel IGBT device is shown in Figure 1. The structure is similar to that of a Vertical Double Diffused MOSFET (VDMOSFET) with the exception that a p–type heavily doped substrate replaces the n–type drain contact of the conventional VDMOSFET (see Figure 2). The p–type substrate is the emitter of the bipolar transistor and is the anode terminal of the device. When sufficient gate voltage is applied, the current that flows at the surface of the MOSFET channel enters the low doped epitaxial layer and appears as a drain current at the substrate. In turn, the heavily doped p+ substrate injects minority carriers into the low doped n– epitaxial layer. The large n– area is needed in order to block high voltages, but it contributes to a large on–state resistance. But the minority carrier injection by the p+ substrate serves to reduce this resistance and thus modulates its conductivity. The injected minority carrier density is typically 100 to 1000 times higher than the doping level of the n–type epitaxial drift region.

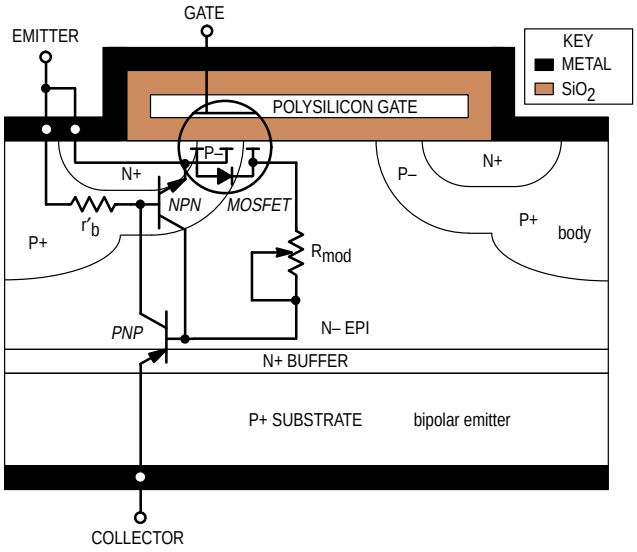

Figure 1. Basic Structure of IGBT

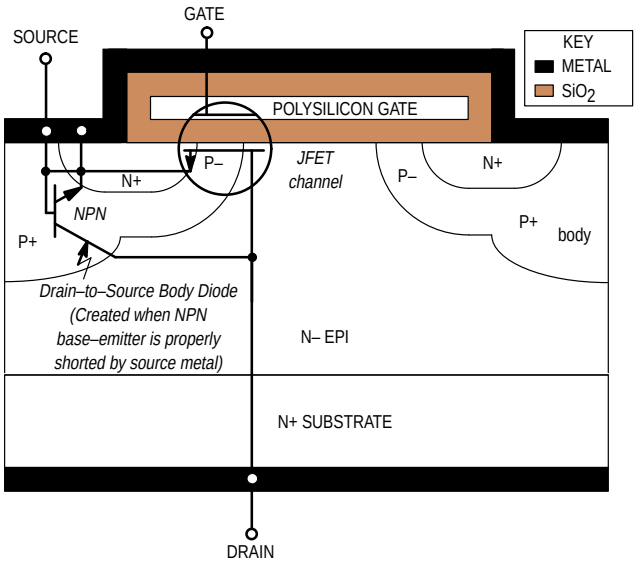

Figure 2. Basic Structure of VDMOSFET

The minority carriers, which do not recombine as they diffuse towards the body, are collected by the body–epitaxial layer which is reverse–biased in the forward conduction operation. The MOSFET channel is formed under the gate where the body meets the silicon surface, and this MOSFET provides the electrons (majority carrier) for recombination in the epitaxial layer and some are injected into the p–substrate region (bipolar emitter). The n+ buffer layer is introduced for the following reasons (we will not discuss it in detail in this paper):

1. Limit injection of holes into n– region. This makes faster devices, but trades off forward drop.
2. Creates low lifetime region for recombination. This only affects speed of non–irradiated devices.
3. Prevents punch–through of depletion region to p+ substrate. This allows thinner epitaxial to be used which lowers $V_{CE(on)}$.
4. Reduces PNP bipolar transistor gain which improves latching and prevents thermal runaway of leakage current at high temperature
5. Sets breakdown voltage of back junction

Much of the discussions presented have been EPI type or “punchthrough” IGBTs because the basic understanding of the device centers around the EPI type IGBTs.

IGBT Equivalent Circuit

The simplified equivalent circuit representing the internal structure is shown in Figure 3. The circuit consists of an N–channel MOSFET, a PNP bipolar transistor, an NPN bipolar transistor, and a JFET. (This is a conceptual model and should not be confused with the actual physical structure of the IGBTs.) The JFET is formed where the MOSFET current flows between two adjacent body diffusions [1]. This JFET supports most of the voltage and is highly modulated giving the MOSFET its low $R_{DS(on)}$. This JFET is represented by the modulated resistor Rmod.

As shown in the model, the bipolar PNP and NPN form a four layer npnp structure of an SCR. If the gains of both transistors are significant enough, the BJTs will latch on and behave just like an SCR. But this latching process is avoided by the base–emitter short resistance, r'_b, in the equivalent circuit. This resistance acts as a shunt to the base–emitter junction of the NPN thereby preventing the NPN bipolar transistor from turning on strongly enough to start the latching process.

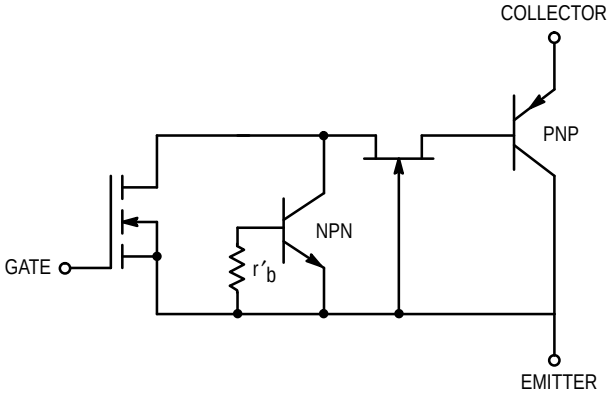

Figure 3. IGBT Detailed Equivalent Circuit Showing the Parasitic Components

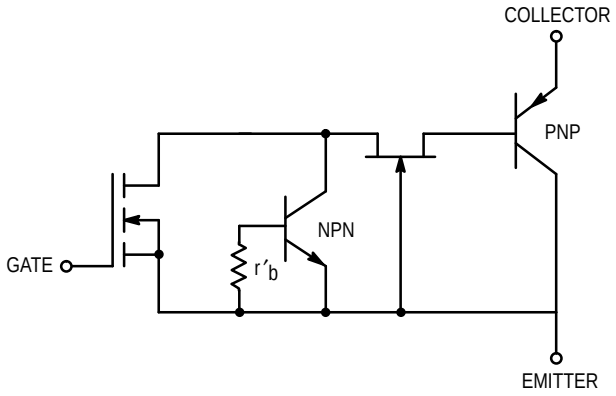

Figure 4. IGBT Detailed Equivalent Circuit Showing the Parasitic Components

Since the current to the base of the NPN bipolar transistor is bypassed, it can be assumed to be off, and this assumption results in the more simplified equivalent circuit as seen in Figure 4. This equivalent circuit only consists of a PNP bipolar transistor and the N–channel MOSFET. The simplified equivalent circuit clearly shows that the drain current of the MOSFET (electron current) supplies the base current of the PNP. The sum of electron current and whole currents make up the total collector current of the IGBT device.

ADVANTAGES OF IGBT

Ease of Gate Drive

As discussed previously, the IGBT combines the best features of the devices mentioned. It uses the low–power, voltage–driven gate drive to turn on and turn off, and possesses a gate impedance as high as that of the power MOSFET.

The structure of IGBT also reduces the reverse transfer capacitance, C_{res}, because a smaller chip area is required for a given current rating. This smaller capacitance results in a very low gate drive power requirement, since only a small gate–drain capacitance charging and discharging current is required (this is one of the real benefits of the IGBT).

Low Conduction Loss

The conductivity modulation of the n– layer greatly increases the current–handling capability of the IGBT for a given die size. This conductivity modulation has been shown to increase the forward conducting current density at given anode voltage up to 20 times that of an equivalent MOSFET and five times that of a BJT [2]. Because this process reduces the on–resistance of the device, the conduction loss is minimized. The disadvantage of conductivity modulation is the increase in device switching time compared to the MOSFET due to stored charge in the wide base region.

Positive Temperature Coefficient

The IGBT also has a favorable temperature coefficient for on–resistance. At **high currents** the on–resistance increases with increase in temperature, and thus the device will not experience the thermal runaway which occurs in the power BJTs. (Note that under nominal and lower collector current range, the devices do have negative temperature coefficient.) It was shown that with increasing temperature, the current sharing of the devices in parallel operation is improved [3].

No Internal Anti–parallel Diode

This can be advantageous or disadvantageous. With the absence of antiparallel diode which is present in power MOSFETs, IGBT can block reverse voltage (approximately –20 V); and with the use of series diode, reverse blocking capability can be greatly increased. The absence of this anti–parallel diode protects the IGBT from reverse conduction problems in the free–wheeling diode, which can occur in power MOSFETs. The designer has the freedom of selecting the optimum rectifier if it is needed in a freewheeling application.

DISADVANTAGE OF IGBT

Current Tail

Even with many favorable qualities, the IGBT device possesses a few unwanted characteristics; one is the slow switching speed as compared to the power MOSFET. When the device operates in forward conduction, the high resistance region n– epitaxial layer is highly modulated with injected excess minority carriers (conductivity modulation). When the gate voltage is removed, this excess of minority carriers must be removed before the device stops conducting completely. The turn–off speed of the device is determined by the integral bipolar open–base charge decay, and results in unwanted current tail (see Figure 5). This slow switching contributes to a large switching energy and limited operation frequencies. The turn–on time is very fast and is determined by the rate of on–voltage saturation of the integral PNP bipolar transistor.

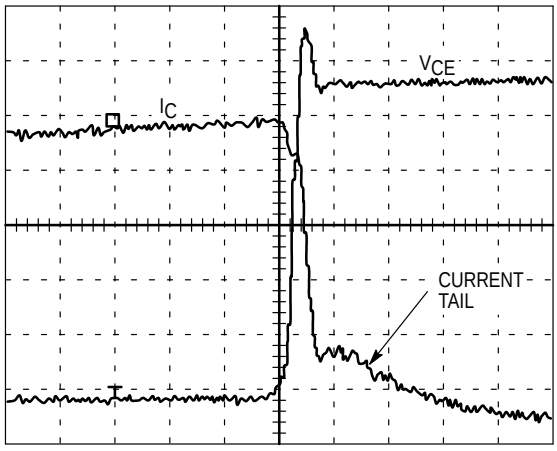

Figure 5. IGBT Turn–Off Waveform

CONCLUSION

The IGBT is a new power semiconductor device which possesses the best features of the both the MOSFET and bipolar transistor. The device is controlled by the same low–power, voltage–driven gate as for the power MOSFETs, and the current handling is similar to that of BJTs. When operating in forward conduction, its conduction loss is reduced by the conductivity modulation achieved by the high level of minority carrier injection from emitter toward the wide base region of the device. It has been shown that the current density is 20 times that of power MOSFETs and five times that of BJTs.

One disadvantage is the current tail during turn–off, and this introduces higher switching losses and limits the operating frequency of the device. At present, frequency of 25 kHz is obtainable without any special resonant switching technique.

IGBT GATE DRIVE CONSIDERATIONS

INTRODUCTION

Devices such as BJTs and thyristors require complicated and very inefficient methods of driving the devices due to their low gain and minority carrier device characteristics. In addition, SCRs become difficult to control due to loss of gate control during turn–off. But it is well known that MOSFETs have the simplest gate drive requirements of all the power devices mentioned. The device can be driven with low power, voltage pulses of required polarity. This simplifies the circuit design, and the switching characteristics can be accurately controlled if all of the circuit parameters are well known.

Because IGBTs are much like fast MOSFETs during the switching transitions, and these devices undergo high voltage and high current transitions, its switching characteristics must be understood by the design engineers in order to avoid some of the problems associated with high voltage and high current transitions. In order to give design engineers a thorough overview of the device characteristics, this section reviews some of the switching characteristics within the clamped inductive load circuit. It is shown that the gate drive circuit, circuit layout, and external components play a vital part in controlling the device switching under clamped inductive load. By understanding the device characteristics and the problems associated with rapid di/dt and dv/dt, the designer can avoid some of the common problems.

This paper covers some of the fundamental switching characteristics, and shows how critical the gate drive circuit is in determining the switching characteristics of the IGBTs. Some of the problems associated with rapid di/dt and dv/dt are discussed, and suggestions are presented in order to overcome these problems.

The parameters that aggravate the problems associated with high di/dt and dv/dt have been shown to be DC bus inductance, common emitter inductance (common to gate drive circuitry), large gate return loop area, the series collector inductance, and the antiparallel diode of the clamped inductive load. All of these parameters contribute significantly to the durability and longevity of the devices, and can affect overall system efficiency.

TURN–ON

Because the IGBT is a MOS–gated device, the turn–on switching performance is dominated by the MOS structure of the device. Figure 1 shows the clamped inductive load circuit used to analyze the switching characteristics of the IGBT. It is assumed that the inductor initially has a constant steady state current flowing through it, freewheeling through the diode. The inductance Ls is the series parasitic inductance due to the power trace and any wiring between the IGBT's collector and DC bus. The inductance Le is the common emitter inductance seen by both the power return and the gate return.

Ideal switching waveforms describing the clamped inductive load circuit are shown in Figure 2. During the time period t0, the gate current charges the constant input capacitance (C_{ies}) with a constant slope, and as is the case with the MOSFET, nothing happens until the gate–source voltage is raised to the threshold voltage V_{th} of the device. During t1, the collector current is redirected from the diode into the device and increases to its steady state value. The current slope is dependent on gate voltage rise time and device forward transconductance. The following expression can be used to express the current slope:

$$\frac{dI_C}{dt} = gm \frac{dV_{GE}}{dt}. \quad (1)$$

The time rate of change in gate–emitter voltage during t1 period is given by:

$$\frac{dV_{GE}}{dt} = \frac{(V_{GG} - V_{plateau})}{R_G \cdot C_{ies}}, \quad (2)$$

If we substitute equation 4 into equation 1, the rate of change of collector current is expressed as:

$$\frac{dI_C}{dt} = gm \frac{(V_{GG} - V_{plateau})}{R_G \cdot C_{ies}}. \quad (3)$$

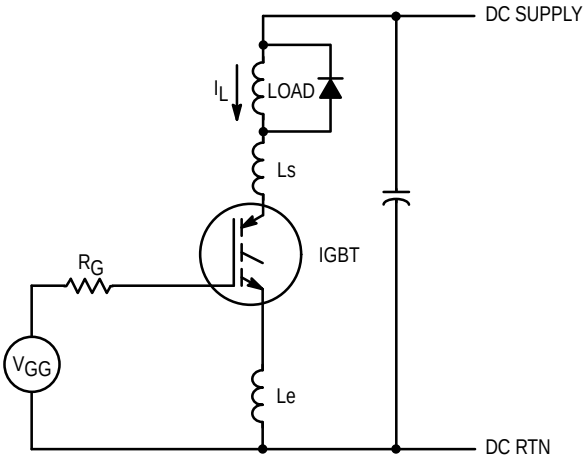

Figure 1. Clamped Inductive Load

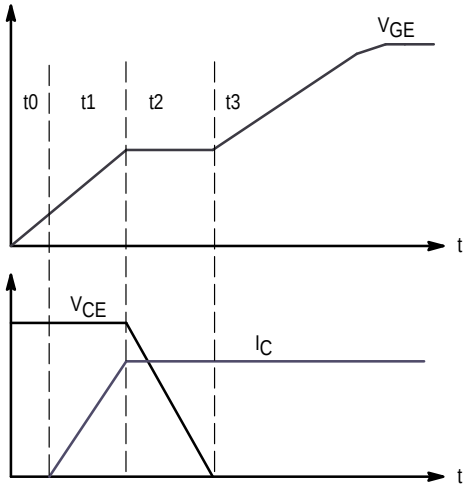

Figure 2. Idealized Turn–on Switching of IGBT

During the plateau region t2, the gate–emitter voltage has reached the value which will support the steady state collector current, and the collector–emitter voltage starts to decrease. During this region, gate drive current is discharging the voltage–dependent reverse transfer capacitance at a constant gate current that can be expressed as:

$$ig = \frac{(V_{GG} - V_{plateau})}{R_G} = C_{res}\frac{dV_{CG}}{dt}. \quad (4)$$

where, $$V_{plateau} = V_{th} + \frac{I_C}{gm}, \quad (5)$$

and gm is the forward transconductance of the device at the given steady state collector current I_C and can be obtained using the transfer curve provided by the data sheets. Transconductance is determined by steady state collector current divided by the intercepting gate voltage (I_C/V_{GE}, see Figure 3). It should be noted here that the above analysis ignores the change in bipolar current gain as base charge is supplied.

The parameter for input capacitance C_{ies} can be obtained using the capacitance curve provided by the device vendors. Figure 4 is a sample curve indicating the capacitance values for input, output, and reverse transfer capacitance C_{res}. A better method of obtaining the capacitance would be to use the gate charge transfer curve. By using the amount of charge needed to turn the device on at a certain operating point, more accurate assessment of gate drive current can be determined. A sample of a gate charge curve for an IGBT is shown in Figure 5, but for qualitative results the curve given by Figure 4 is adequate.

All of the above expressions are presented to show the relationship between the series gate resistance and its effect on the rise time of the device current. Using these equations, the designer can control the current and voltage slope during turn–on. During region t3 the dynamic switching is completed, and a further increase in gate–emitter voltage has no effect on the dynamic characteristics. But, as we will discuss later, the final gate–emitter voltage determines how much turn–on loss is expended by the circuit and determines the magnitude and duration of short circuit current handled by the device.

Turn–On Switching Considerations

In order to reduce the dynamic turn–on loss, the switching time must be very short. This requires that the gate drive be a low impedance type, and be able to provide a large narrow pulse of current to charge the input capacitance which includes the feedback capacitance and gate–emitter capacitance. The turn–on switching time is determined by how quickly the input capacitance C_{ies} is charged. However, the fast switching speed will introduce high di/dt (maximum di/dt is a function of load inductance and the gate drive: 1) where initial di/dt = V/L, and once inductance has charged to its maximum load current, 2) the di/dt will be dominated by the gate drive) which will interact with the lead inductance of the emitter. The control of turn–on di/dt can be seen by observing equation 5. In this equation it is evident that by changing the gate resistor value, the rate of the rise of the device current can be increased. This large di/dt will induce large enough transient voltage across the common emitter inductance and will reduce the available gate voltage causing linearization of the initial collector current rise because of its gate current limiting while increasing the turn–on loss [4]. In order to overcome this problem, a small gate resistance is placed in series with the gate of the device, but remember that the inductance seen by the gate must be minimized. Placing the components as near as possible to the gate–emitter terminals, along with good circuit layout, will reduce much of the unwanted inductance. Also, the gate–emitter current loop must be short. It is good practice to use twisted wire or parallel power paths. Overlapping the power and return paths of the gate drive has the advantage of nullifying magnetic field induced by power trace with the magnetic field induced by the return trace and the effective loop inductance is minimized.

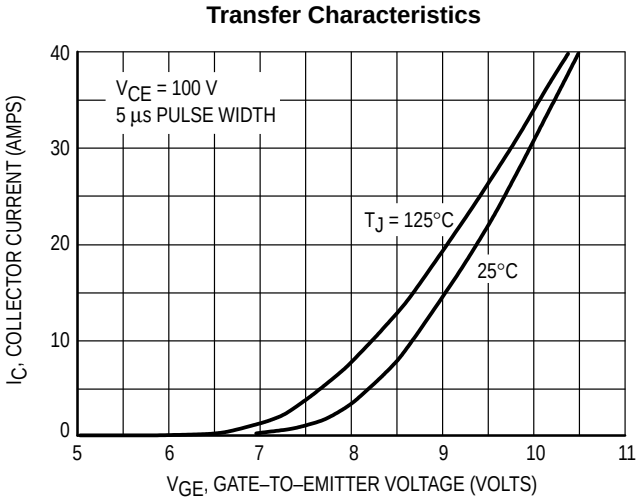

Figure 3. Gate–Emitter Voltage Due to Temperature Variation

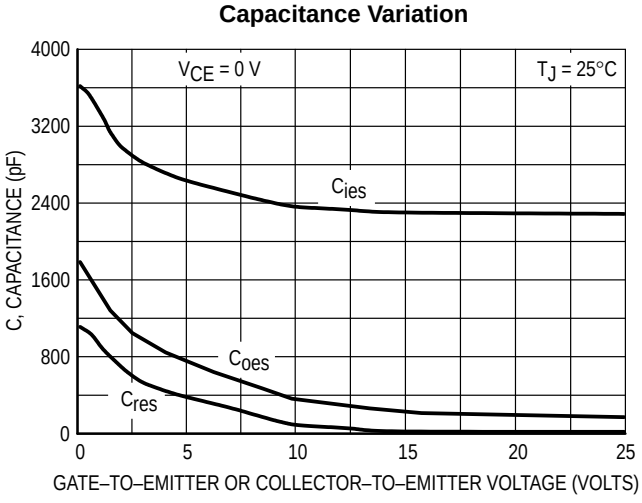

Figure 4. IGBT Capacitance Curves

Gate–to–Emitter and Collector–to–Emitter Voltage versus Total Charge

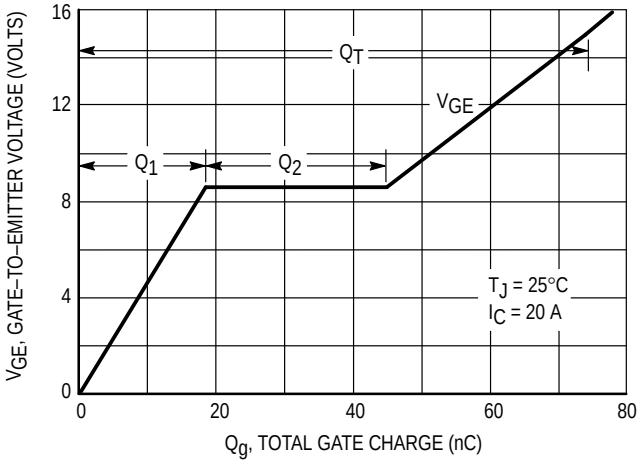

Figure 5. Gate Charge Transfer Curve

Rapid di/dt not only limits the available gate voltage, but causes the bus voltage to dip, or decrease due to Ls(di/dt), where Ls is the stray inductance of the power DC bus. During turn–off, the rapid di/dt will cause a large positive voltage to be seen by the device which can exceed the rating of the device. Therefore, it is important to reduce di/dt during turn–on and turn–off duration. A local bypass for the DC bus should be provided as near as possible to the device with a high current, low ESR capacitor. Without these precautions the IGBT may encounter avalanche breakdown due to di/dt induced transient during the turn–off time.

Effect of the Freewheeling Diode

Just as during turn–off, a surge can occur during the recovery of the freewheeling diode. For high di/dt, the reverse recovery of the diode can become very snappy. Because of the stray inductance within the circuit and the device leads, this large di/dt will cause a large dv/dt once the diode is recovered. The high di/dt caused by the snappy recovery of the diode can cause large unwanted voltage transients. Therefore, proper choice of the freewheeling diode is absolutely critical in the performance of the device. A snappy recovery can be controlled or eliminated by increasing the gate resistance R_G, but this will increase the turn–on time, and the efficiency of the circuit will suffer. Therefore, an ultrafast diode with a soft recovery must be chosen. Otherwise a snubber must be used to control the snappy recovery of the diode.

TURN–OFF

The turn–off of the IGBT is initiated by removing the voltage across the gate–emitter just as for MOSFETs. Figure 6 shows idealized turn–off waveforms for switched inductive load. The first part of the turn–off process is the delay time ($t_{d(off)}$), which is the effect of the time required for the gate drive to pull V_{GE} from its full value to the level at which the collector voltage begins to increase. Nothing is observed while gate voltage is decreased, until the gate voltage reaches the value required to keep the collector steady state current to flow. During t5, the collector voltage rises, and its rate of rise can be controlled by the gate resistance R_G:

$$\frac{dV_{CE}}{dt} = \frac{V_{plateau}}{C_{res} \cdot R_G}. \quad (6)$$

Equation 6 assumes that the gate resistance is large enough that the output capacitance is not the limiting factor.

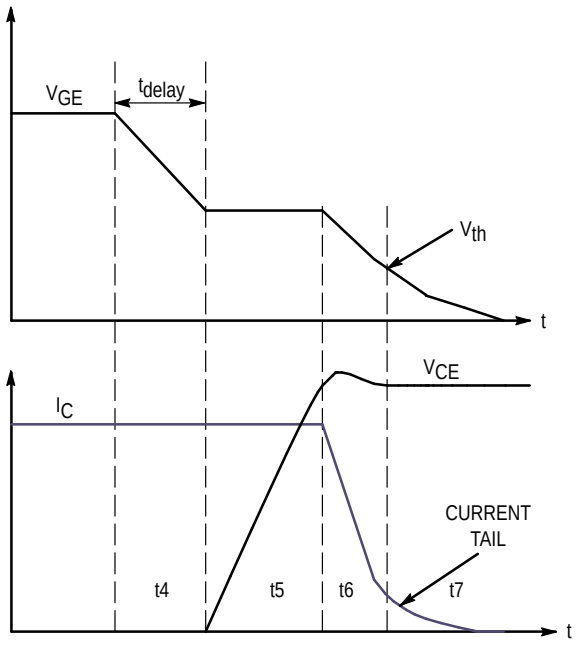

Figure 6. Idealized Turn–off Switching for IGBT

At t6, the collector voltage has reached the bus voltage V_{DD}, the freewheeling diode starts to conduct, and collector current starts to decay. Because of the high di/dt, the collector voltage rises beyond the bus voltage due to L(di/dt) overshoot. The region, t6, is the initial fall time, and this is the time required for the gate drive circuit to remove the charge that flows into the gate from the gate–to–drain capacitance as V_{DS} increases during turn–off. This period is greatly influenced by the gate drive design and its drive impedance, R_G. For small gate resistance, period t6 is determined by the clamp inductance. This period is defined as the time it takes for Ic to drop from 90% of its full current down to approximately the 10% level (this will include the tail). This period is greatly influenced by the gate drive design and its drive impedance, R_G, and the effect of R_G on the collector current fall time is expressed as:

$$\frac{dI_C}{dt} = \frac{V_{plateau}}{R_G \cdot C_{ies}}. \quad (7)$$

The time period t7 shows an abrupt decrease in current slope. This current slope is due to the recombination of the minority carriers in the wide base region of the integral BJT. This recombination process produces what is frequently termed as the “current tail.” This current tail limits the operation frequency of the IGBTs, and the size and length of this current tail is determined by the device design and process technology.

Turn–Off Considerations

Just as with the MOSFETs a negative bias can be applied to the gate in order to speed up the turn–off. This does not mean that the recombination of minority carriers in the wide base region will be increased, but it helps to speed up the turn–off of the MOSFET portion, and thus turns off the base of the integral PNP bipolar transistor quicker. The rapid turn–off will cause a high dv/dt.

The problem associated with high dv/dt is that it can introduce current through the capacitance to the base of the internal parasitic NPN bipolar transistor (only in a bad device), thereby causing the device to latch on. Once the device is latched on, the gate–control is lost and the device cannot be turned off without removing the power to the collector terminal of the device (see Figure 2). A small gate–emitter resistance can be added to the terminals to bypass the dv/dt problem. Also a series resistor should be used when negative gate bias is applied during the turn–off process. The negative bias should be left on while the device is turned off. This will protect the device from the false turn–on due to the dv/dt problem. Optimum values of the resistors can be found by trying different values of the resistor in the circuit to be used or by simulation.

Effect of the Current Tail

The t7 interval, as discussed earlier, is a result of minority carrier recombination in the bipolar PNP structure. IGBT is a minority carrier device during the forward conduction, and as such the highly resistive region (n– epitaxial layer) is highly injected with minority carriers. This minority carriers must be removed before the device stops conducting completely. The turn–off speed of the device is therefore determined by the integral bipolar open base turn–off. This tailing effect is the direct result of the internal base of the PNP structure which cannot be accessed by the external means; and as a result, we cannot discharge the excess minority carriers by reverse biasing the gate. The controlled rate at which the minority carriers recombine is a function of device design and process technology. This current tail contributes to limit operational frequency and introduces large switching energy to be dissipated by the device. How fast the minority carriers recombine determines how long the current tail is and the turn–off speed of the device.

GATE DRIVE REQUIREMENTS

From the previous discussion of switching characteristics of the IGBT, the following have arisen as the important factors that need to be considered when designing the gate drive:

1. Reduce the gate–emitter current loop by separating the power return and gate return
2. Use a twisted wire if possible and overlap the power traces of gate drive if PCB is used
3. Make the gate drive connection as short as possible to the device being used so as to reduce any parasitics
4. Use a series gate resistor, R_G to limit di/dt and dv/dt
5. Use a negative bias if possible to reduce any dv/dt problems

CONCLUSION

IGBTs are excellent candidates for high power applications. However, when switching high voltage and high current, care must be taken in the beginning stage of the design to ensure that circuit layout will support the high di/dt and dv/dt. Some equations have been provided so that by using appropriate gate resistors, di/dt and dv/dt can be controlled.

It was observed that the gate drive is a vital element in obtaining the maximum performance of the device. Through the correct use of gate drive the designer can overcome some of the common problems associated with high voltage high current switching: 1) accurately control di/dt and dV_{CE}/dt problems, and 2) avoid latching of the parasitic thyristor. Using a negative bias at the gate reduces the chance of false turn–on and latching of the device. Not only was the gate drive vital in determining the switching loss, but the freewheeling diode in a clamped inductive load introduces turn–on switching losses. It is of utmost importance that an ultrafast diode with soft recovery type be chosen.

Layout of the circuit was vital in overcoming some of the switching problems. The ground loop of the gate drive must be separated from the power return so that the common emitter inductance does not interrupt the turn–on process. The twisted wires or parallel power tracts should be used for the gate drive. In order to reduce any unwanted supply bus inductance, it was suggested that a bypass capacitor with low inductance and low ESR be connected right at the device level, or just as in gate drive, the supply bus tracks can be paralleled. By following some of these recommendations, many of the common problems associated with high current and high voltage switching can be dramatically reduced.

EFFECT OF GATE–EMITTER VOLTAGE ON TURN–ON LOSS AND SHORT CIRCUIT CAPABILITY

INTRODUCTION

Unlike the MOSFETs and BJTs, the magnitude of the gate–emitter supply voltage of an IGBT has a significant impact on the performance of the device. The magnitude of the gate voltage impacts the turn–on loss and short circuit survival capability of the devices. In this section some of the impacts of the gate–emitter voltage on the device performance will be examined.

TURN–ON LOSS

As mentioned before, the turn–on characteristics of IGBTs are similar to those of a MOSFET. In MOSFETs, once the gate–source voltage has reached the value to support the steady–state drain current, a further increase in V_{GS} has no significant role in the circuit, but it does greatly affect the switching speed of the device. The magnitude of the gate–emitter voltage significantly affects the magnitude of the turn–on loss during the transition.

Figure 1 depicts measured data that shows the relationship between gate–emitter voltage and turn–on loss with a constant R_G, 20 ohms. As shown by the curves, larger gate–emitter voltage reduces the turn–on loss of the device. This can be explained by the fact that for a given gate resistor, the gate current available increases with the increase in the gate voltage. Therefore, the input capacitance of the device is charged at a faster rate which can account for less loss. The longer it takes the device to turn on, the more energy is dissipated by the device. For given collector currents, increase in gate–emitter voltage reduces turn–on loss.

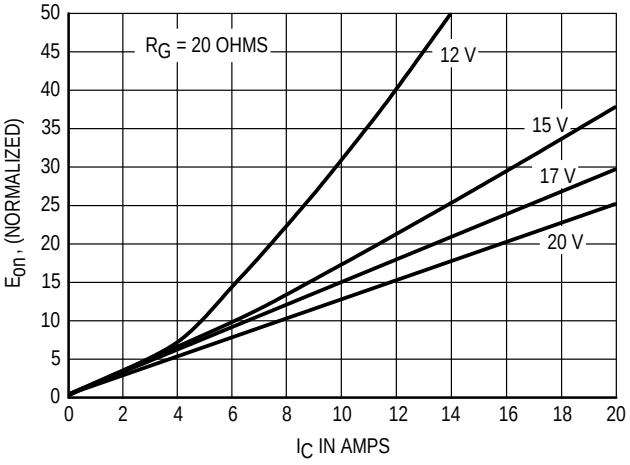

Figure 1. Turn–on Loss with Different Gate–Emitter Voltage

SHORT CIRCUIT FAULT OPERATION

A major concern in inverter applications is the ability to survive a short circuit fault condition. During the short circuit fault, the device is exposed to the supply voltage across the device, while the gate potential is at full operating value (see Figure 2). Because of the high gain characteristic of the IGBTs, the collector current will rise to some undetermined value limited by the gate–emitter voltage. During this time the device will have a large amount of energy across the device, and if the energy is beyond the capability of the device it will be destroyed due to thermal breakdown. For the bad devices, the large current can cause parasitic NPN bipolar transistor to turn on and cause the device to latch, wherein the gate control will be lost.

One point to note here is that the IGBTs are less sensitive to second breakdown due to hot spot formulation unlike the BJTs. In understanding this, it is clear that the device should be able to survive a short circuit condition if the energy delivered to the device is maintained below some value that is tolerable to the device.

There are many different ways to protect the device from the short circuit condition for some duration. Remember that the device does not turn off when a short circuit occurs, but rather limits the amount of the energy dissipated by the device by limiting the collector current. This provides enough time for the external protection circuits to be activated. Therefore it is of utmost importance that the device be able to survive a short circuit fault condition. The most effective way to provide the short circuit survivability would be to inherently build current sensing capability into the device, but as of now, no manufacturer has any device which has built–in current sense for short circuit detection. IGBTs produced by Motorola are capable of short circuit survivability of 10 μs minimum.

Another method of increasing the short circuit survivability is to decrease the gate voltage when the short circuit across the device is observed. Figure 3 data shows the relationship between the gate voltage, short circuit current, and the short circuit survival time period. As shown in Figure 3, it is clear that the smaller gate voltage limits the current at lower value and increases the short circuit time duration.

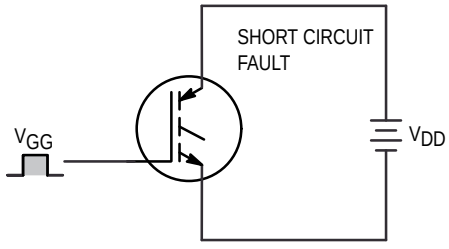

Figure 2. Equivalent Short Circuit Condition

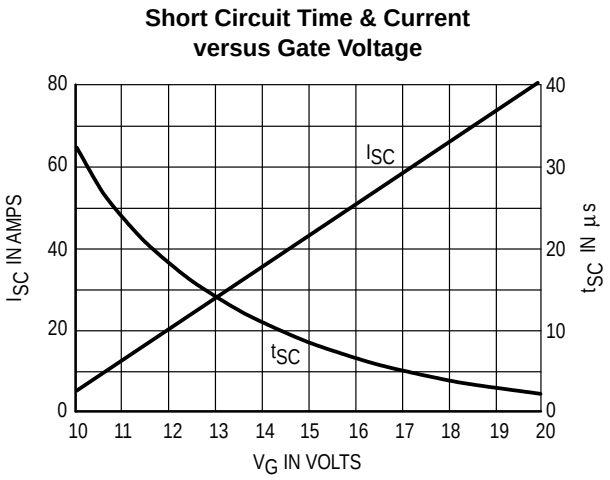

Figure 3. Short Circuit Response of IGBT

SUMMARY

IGBTs are high current and high voltage devices. Because of their use in high power applications, it is important that some of the key behavior of the device is understood by the user in order minimize switching losses and to prolong their lifetime.

In most cases, the turn–on loss of the device in a clamped inductive load is dependent on the performance of the free–wheeling diode, and is a function of the diode's reverse recovery time. But as we have discussed, the magnitude of the gate–emitter voltage can be optimized in order to reduce the turn–on loss of the device. But on the other hand, the designer needs to understand that the high gate–emitter voltage reduces the short circuit survivability of the device.

Using these two relationships, the designer can choose the best voltage value which will meet their design requirements.

FORWARD CONDUCTION AND TURN–OFF BEHAVIOR OF IGBTS AT HIGH TEMPERATURE AND ITS CONTRIBUTIONS TO STATIC AND DYNAMIC TURN–OFF LOSS

INTRODUCTION

IGBTs have been introduced to overcome the high on–state voltage of MOSFETs and slow switching frequency of BJTs. But because IGBTs possess dual device characteristics, their behavior is not easily understood. In high current applications, the on–state voltage becomes a major issue, and, in other cases switching losses may be the major concern. In this section the on–state voltage characteristics and dynamic turn–off will be discussed. It is shown that the unique characteristics of the IGBTs allow the designer to operate the device to obtain low conduction loss. But also shown are that dynamic turn–off losses must be taken into consideration with variation in temperature.

During the turn–off at high temperatures close attention must be given to: 1) current tail variation, 2) initial current height of the anode current, 3) reduced rate of rise of anode voltage, 4) and increased carrier lifetime. All of these add to the turn–off energy loss and can damage the device if care is not taken.

FORWARD CONDUCTION

Because IGBTs behave like MOSFETs in switching transitions, it can be misunderstood that the device always possesses a positive temperature coefficient (that is, the on–voltage increases at higher temperature). This perception is partially correct. As we shall see the device actually possesses negative temperature coefficient at low current levels.

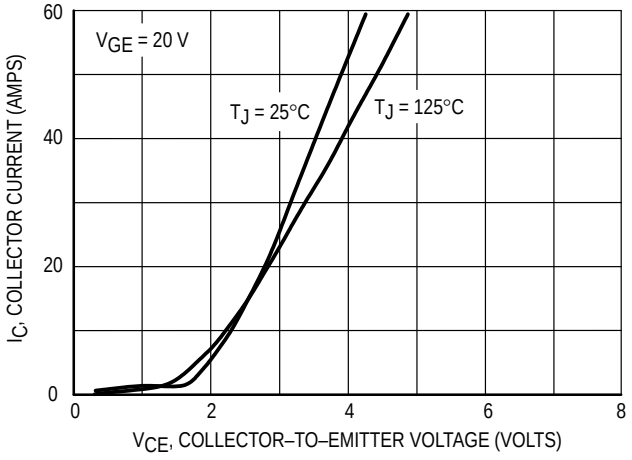

Figure 1. IGBT Output Characteristics

IGBTs possess aspects of both MOSFET and BJT characteristics. Figure 1 shows the temperature dependence of collector current versus collector–emitter voltage. For low current levels, the device possesses a negative temperature coefficient, and as a result the saturation voltage is decreased with increase in temperature. At some current level, the two curves cross each other and at this crossover point V_{CE} becomes temperature independent. At higher current levels, the device possesses a positive temperature coefficient characteristic and its saturation voltage increases with increase in temperature.

At high temperature, there are a few important things that are happening which contribute to the device on–voltage. It was discussed by Hefner [5] that: 1) the base resistance increases with temperature due to decrease in the mobility of the carriers, 2) emitter–base junction diffusion voltage decreases due to increase in base intrinsic carrier concentration, 3) the drain–source voltage increases slightly with temperature because the decrease in MOSFET transconductance dominates the decreasing threshold voltage for the high gate voltage bias condition.

The on–voltage of the device decreases with temperature at lower current levels because the base resistance and channel resistance is small compared to the change in emitter–base junction diffusion voltage. The BJT characteristics of the device are dominating at this point. But for higher current levels, the base resistance and channel resistance start to become significant enough and dominate the on–voltage of the device, and as a result, introduce the positive temperature coefficient which is a MOSFET effect of the device.

If the operating current is within the negative temperature coefficient region, one can be mistaken in thinking that operating the device at a higher temperature will be much more efficient. This may be true if other factors such as conduction current, thermal environment, circuit layout, and other operating parameters have been considered. But as we will later see, dynamic turn–off must be considered at high temperature operation

TURN–OFF

Unlike the relatively temperature insensitive forward voltage drop of the device, the turn–off energy loss is increased with temperature. Figure 2 shows the dramatic increase in turn–off loss at high temperature. This increase in energy loss is contributed largely by the increase in the current tail. The current tail is a function of the base minority carrier lifetime and is increased with rise in temperature. Not only is current tail length increased, but the storage time, dV_C/dt, and initial anode current tail height is also increased. These effects all contribute to higher turn–off energy loss, and attention should be given by the designers using the IGBTs. By understanding how the device behaves with the temperature at turn–off, the design engineer can better assess the best operating parameters for a given application.

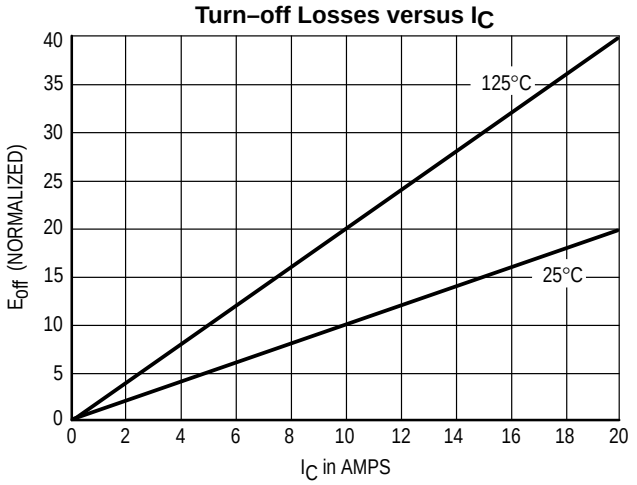

Figure 2. Turn–off Energy Loss at Different Temperatures

Current Tail

With an increase in temperature, the mobility of the minority carriers in the wide base is reduced, and the lifetime is increased which prolongs the current tail during the turn–off of the transistor. The increase in the current tail can account for almost 60% of the turn–off loss. Not only is more energy dissipated by the device, this will reduce the operating frequency of the device. Figure 3 depicts the anode current during the turn–off. The initial current height is denoted by $I_T(0+)$ and is the time at which the current tail starts to decay exponentially. For devices which do not have the buffer layer, the initial height of current tail remains relatively constant and with temperature only current tail length is increased. But for devices with the buffer layer, this initial tail height increases with the temperature. Both the increased height and length of tail with temperature means that the device will turn off slower.

It was discussed that the $I_T(0+)$ is proportional to the base charge Q, and diffusivity of the device [6]:

$$I_T\,(0+) \propto Q \cdot D \qquad (1)$$

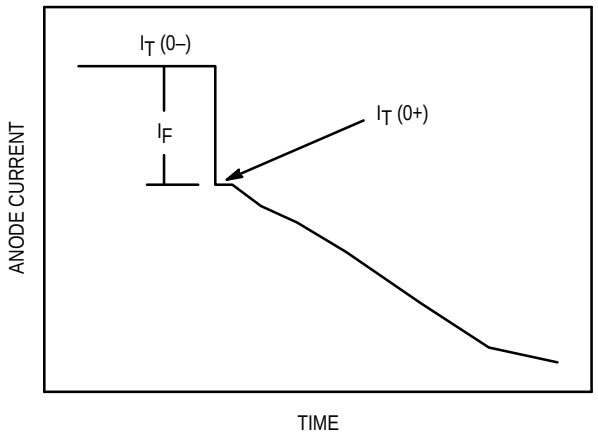

Figure 3. Anode Current During Turn–off

For nonbuffered devices, the increase in the base charge with temperature is negated by the corresponding decrease in the diffusivity. But in the buffered devices, the increased charge due to the temperature is greater than the decrease in the diffusivity of the device, and as a result, the initial current magnitude varies with temperature. The variation in initial current height and in current tail length is the major contributor to the turn–off energy loss.

Figures 4 and 4b show turn–off waveforms at two different temperatures. The data shows that the initial current height and current tail is increased significantly at higher temperatures. This increase in the current tail length and initial current height contributes to a larger turn–off energy loss.

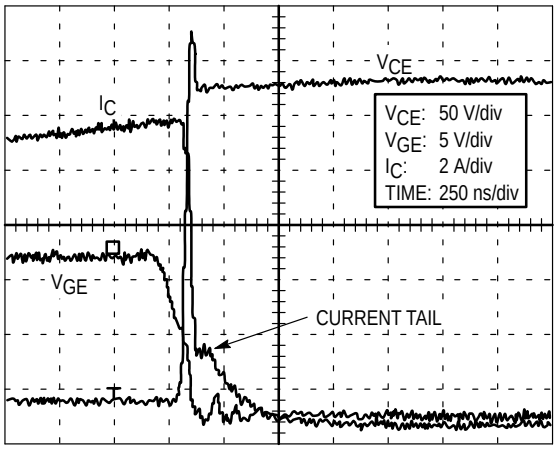

Figure 4a. Turn–off Waveforms at 25°C

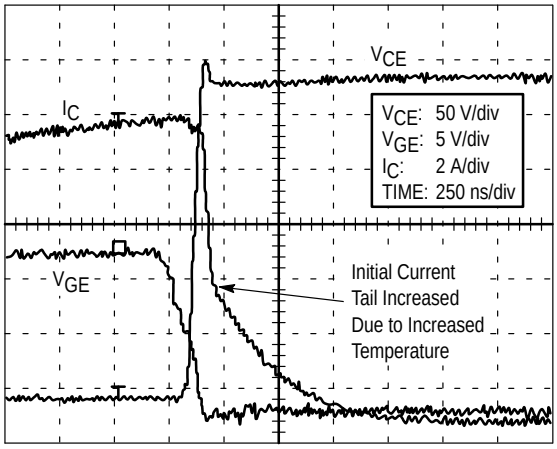

Figure 4b. Turn–off Waveforms at 120°C

Collector Voltage Transitions

In the previous paragraphs it has been discussed how the increase in device temperature decreases the mobility and increases the lifetime of a device. This increase in lifetime also increases the current tail length and its associated initial current height. But as we shall see, the rate of rise of the anode voltage is also affected by the temperature due to increase in the lifetime, and adds to total turn–off loss.

Figure 5 shows an equivalent schematic of IGBT showing all of the internal circuits associated with the device. During the turn–off, the output capacitance is dominated by the collector emitter redistribution capacitance, C_{cer}. This capacitance is orders of magnitude larger than the depletion capacitance and dominates the effective output capacitance of the IGBT during turn–off. Because this capacitance is charge dependent, its value is varied with change in temperature (charge is varied with temperature). At high temperature, the increase in charge increases the effective output capacitance and thus decreases the rate–of–rise of the collector–emitter voltage. The following equation can be expressed as:

$$I_{base} = \frac{Q}{T_{HL}}. \quad (2)$$

Current I_{base} is a steady state current level, charge Q is charge present in the base, and t_{HL} is the excess carrier lifetime. With increase in temperature, the whole lifetime is increased due to reduction of mobility of carriers within the base region. The increase in the base lifetime means that the charge must increase in order to provide the unchanged collector current. During the voltage transition, the effective output capacitance and rate–of–rise of the anode voltage must be able to supply the steady–state collector current. Since the capacitance is proportional to the amount of charge present, its value is increased accordingly. Larger capacitance then decreases the rate–of–rise of the anode voltage because it takes longer to charge the bigger capacitance. The rate–of–rise of the collector voltage is an inverse function of the capacitance, and the following expression can be used to describe its dependency on charge and capacitance:

$$\frac{dV_C}{dt} \propto \frac{1}{C_{cer}} \propto \frac{1}{Q} \quad (3)$$

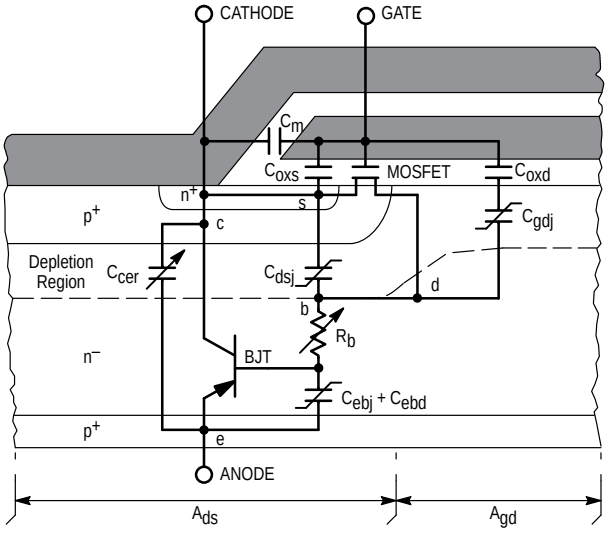

Figure 5. IGBT Equivalent Circuit Superimposed on One–half of Symmetric IGBT Cell (Reprinted with permission from NIST)

Storage Time

Other side effects of the decrease in the rate–of–rise of the voltage is that it prolongs the storage time. In a clamped inductive load, the collector voltage must reach its full supply voltage value before the collector current starts to decay (see Figure 5). The decrease in dV_{CE}/dt causes the collector current to remain at its full steady–state value much longer, and hence increases the turn–off loss.

FURTHER DISCUSSION ON TEMPERATURE EFFECT

Figure 6 shows all of the phenomenon that has been discussed previously. The first thing to note is that the initial current tail magnitude has increased dramatically. But also note that the storage time has been increased due to the decrease in dV_{CE}/dt. As shown in Figure 6, dV_{CE}/dt is decreased by a factor of two, and is independent of gate voltage after t6 region (it is assumed that there is no significant variation in gate drive performance with variation in temperature). Notice the lack of voltage overshoot due to decrease in the slopes.

Figures 7 and 8 are measured data showing the effect of temperature variation during the turn–off. All of the phenomenon discussed are apparent during the turn–off transition. One important factor to remember is that the device was operated only at 50% of its rated voltage. If the collector voltage is increased, the turn–off loss encountered can increase much more which will then increase the junction temperature of the device. (See Figure 9.) So special care should be given to the turn–off transition if the device is to operate efficiently under temperature variations.

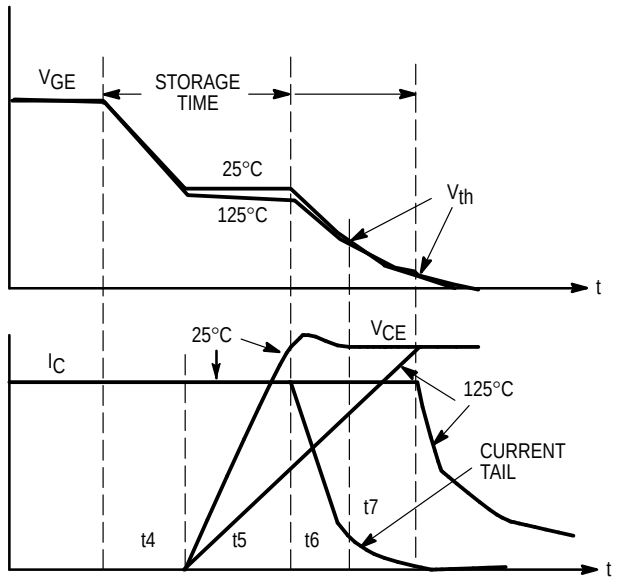

Figure 6. Turn–off Behavior of IGBT with Temperature Variations

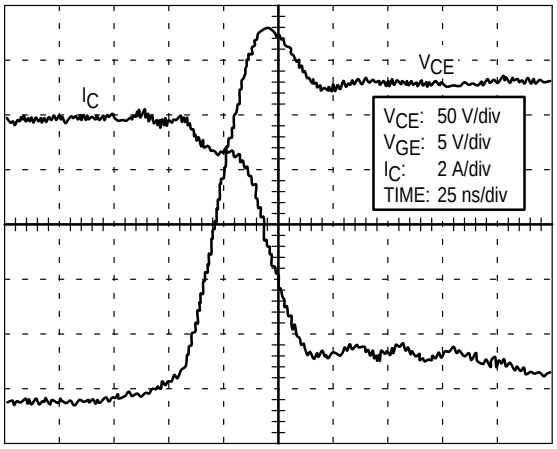

Figure 7. Turn–off at 25°C (V_{DD} = 300 Vdc)

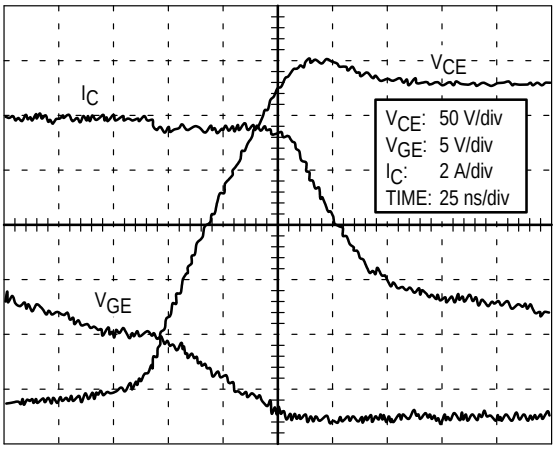

Figure 8. Turn–off at 120°C (V_{DD} = 300 Vdc)

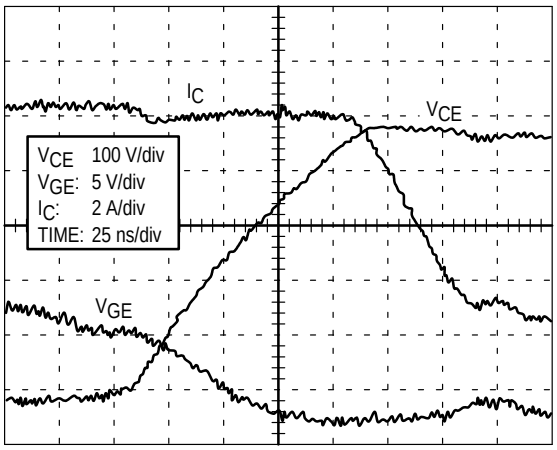

Figure 9. Turn–off at 120°C (V_{DD} = 500 Vdc)

CONCLUSION

IGBTs have very unique characteristics which can be utilized to best meet many of the high power switching applications. But unlike BJTs and MOSFETs, it is not straightforward when it comes to designing for temperature variations. One must not only look at the on–state voltage, but one also needs to consider the dynamic behavior of the device with temperature. How well the device temperature is stabilized determines how rugged the device will be. If the environment is such that temperature variation is minimal (and can be guaranteed), the design can be optimized for the on–state voltage because the turn–off energy loss variations will be small. But if the temperature stability is not guaranteed, the designer needs to consider all of the parameters discussed and great care should be given to device junction temperature. The design should be done by derating the part for the worst case condition which the device will confront. If care is not taken, one can be assured of device failure or degraded performance. The following are some of the considerations that should be taken when using IGBTs:

1. Temperature environment of the circuit
2. Device characteristics with temperature variations
3. Increase of storage time
4. Decrease of dV_C/dt
5. Increase in initial current tail height
6. Increase in total current tail length
7. Operating current of the device
8. Operating frequency

Considering these factors will help the design engineers to better utilize all of the benefits of IGBTs.

IGBT PARALLELING CONSIDERATIONS

INTRODUCTION

Paralleled IGBTs are used extensively in power modules to obtain higher current ratings [3], thermal improvements, and for redundancy. However, the typical process variation of device parameters within a given device type is significant enough to result in uneven static and dynamic current sharing if the paralleled devices are chosen randomly from a given lot of IGBTs of the same type. Design engineers must make sure that the temperature variations do not significantly vary the significant device parameters, and caution must be observed. Aside from the temperature and device parameter variations, it is well known and much has been written about how the circuit layout and its contribution can greatly influence the performance of devices in parallel operation.

In this section the characteristics of IGBTs under parallel operation are shown. The effect of device parameter variations under static and dynamic current sharing are studied, and the effect of temperature and circuit layout are discussed. Then some suggestions are presented on how to overcome the common problems associated with paralleling IGBT devices. It is shown that if the designer considers careful circuit layout, thermal considerations, and pays careful attention to process variations within the given lots, many of the problems associated with the paralleling power IGBT devices can be avoided.

Many of the papers written about parallel operations of IGBTs concern the effect of temperature variations. It is true that temperature is the key role player in the destruction of IGBT devices. But it is unclear as to what or how the temperature is changing the device characteristics. The IGBTs have the dual device (MOSFET and BJT) characteristics, and in order to truly understand the temperature effect on paralleling, it is necessary to understand how the temperature changes the characteristics of each device type. In this way the designer is better informed and will be able to better design for “key” parameters.

PARAMETER VARIATIONS

In order to observe how the dissimilar parameters affect current sharing of the paralleled IGBTs, the parameters lifetime t_{HL}, threshold voltage V_{th}, and transconductance Kp, were varied between two different devices. These parameters were chosen because the normal process variation of these parameters has the most impact on current sharing for parallel operation [7].

The circuit used to simulate and test the parallel operation of IGBTs is shown in Figure 1.

The inductors LS1, LS2, Le1, and Le2 are the inductances due to lead and power traces. The load resistor RL is used to limit the collector current to a safe level. It is shown that these parasitic components have a significant role in the operation of the IGBTs.

Variations in Lifetime

The effect of lifetime on the IGBT is through the bipolar characteristics of the device. In order to understand how the lifetime variation behaved in parallel operation of IGBTs, two devices with dissimilar lifetimes were observed. Figure 2 shows a waveform of collector voltage and collector current of both device types. The difference in lifetime has no effect on

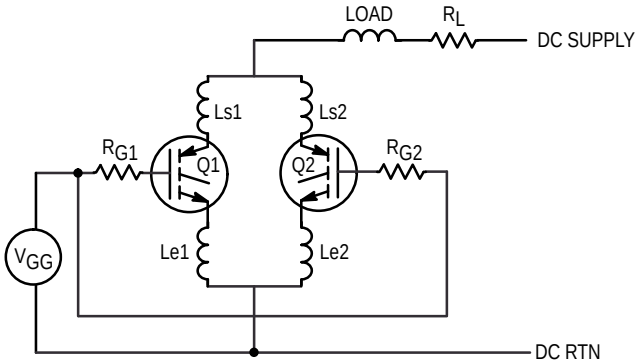

Figure 1. Paralleled IGBTs Used in Inductive Load

turn–on transitions, but the current imbalance during the steady–state region, and turn–off variations are observed. The device with the higher lifetime conducted more current than the device with lower lifetime. Because of this higher lifetime, more charge is stored in the wide base region, and thus decreases the saturation voltage. With its lower $V_{CE(sat)}$, it draws more of the load current. No significant current spike is observed during the turn–off transition, but as expected the device with higher lifetime had a larger current tail because more charge had to be removed.

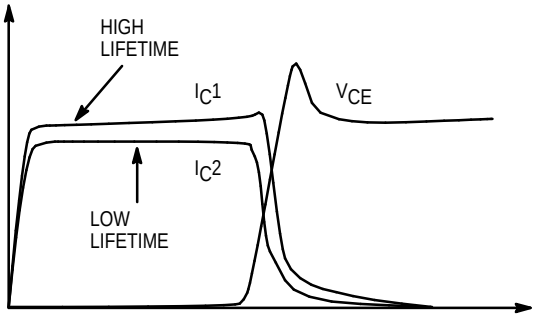

Figure 2. Paralleled Operation of IGBTs with Lifetime Variation

Temperature Effect on the Lifetime Variations. With increase in temperature the lifetime increases. Figure 2 shows that if the static current sharing is within the tolerable region, there is no problem associated due to lifetime variations. During the turn–off sequence, the length of the current tail of the device with higher lifetime is increased. This increase in current tail will increase the turn–off loss of that device but should not have significant effect on the static current sharing if the parameter variation is minimal. But if the devices have wide variation in the lifetime, the device with the higher lifetime can encounter thermal breakdown (for example, paralleling an ultrafast IGBT with a slow IGBT). The thermal effect of the device is overcome by using the same heatsink for both devices and the temperature feedback between the devices will keep the current sharing very constant because the lifetime of both devices will vary together and one will track the other constantly. Because the current tail is the same in a paralleled configuration as for a single device, the destruction

of the device due to life time variation is the same as for single devices used in a scaled down circuit. If the designer did not consider the temperature effect of the current tail, $V_{CE(on)}$, and the energy loss, the device may fail due to excessive energy dissipated by the device at high temperature. However, in a parallel operation, unless a large quantity of the devices are paralleled for very high current levels, the failure of the device in paralleled operation would be the same as in a single device operation.

Threshold Voltage and Transconductance Variation

Threshold voltage and transconductance are MOSFET characteristics. Two devices with different MOSFET threshold voltages and transconductance were chosen, and the resultant waveform is shown in Figure 3. The turn–on delay occurs for the higher threshold voltage device because it takes longer for the gate voltage to charge up the gate–emitter capacitance to its threshold voltage. Not only does the threshold voltage cause the delay, but the lower transconductance will cause delay during the turn–on because the device resistance is higher than the other device until its gate voltage becomes large enough so that the on–state resistance of both devices are primarily determined by the bipolar emitter–base voltages. The static portion of the waveform shows a current imbalance, and the device with the higher transconductance conducts more current because its on–resistance is lower than the other device. At turn–off, a current spike exists for the device with the larger transconductance and smaller threshold voltage. The turn–off current spike in the higher transconductance device occurs because the resistance of the lower transconductance device becomes larger sooner than for the high transconductance device, and the inductor current is transferred to the lower resistance device. The turn–off current spike introduced by variation in transconductance and threshold voltage can be detrimental to the device if its SOA has been exceeded.

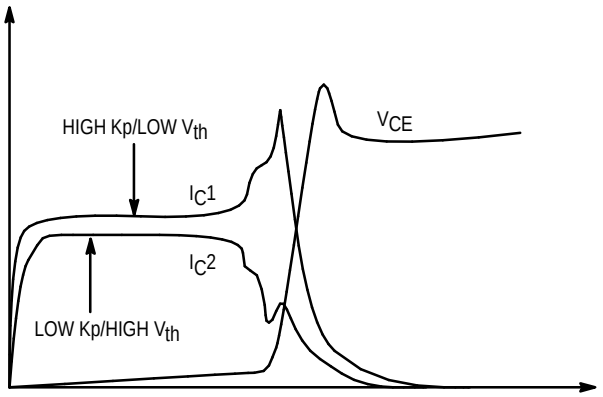

Figure 3. Paralleled Operation of IGBTs with Kp and V_{th} Varied

Temperature Dependency of V_{th} and Kp. With an increase in temperature, both of the parameters will be decreased. For a high–gate voltage, the on–state voltage will tend to increase with temperature, but because the IGBT has dual device characteristics, the BJT emitter–base voltage decreases with temperature due to the increase in intrinsic carrier concentration. The decrease in BJT emitter–base voltage will negate the decrease in transconductance, and as a result, the amount of current seen by the device will be changed very little or not at all. But if the current level is high enough, the MOSFET effect will dominate and the device $V_{CE(sat)}$ will increase with temperature. This increase in on–resistance of the device will cause the other device to take more of the current, and thereby always keep the current–sharing well balanced. Unless the parameters are significantly different, static current sharing is well balanced from device to device.

During turn–off, however, the device with higher transconductance will conduct most of the current because the MOSFET channel resistance dominates during switching. If the variation in transconductance is wide enough, one of the devices can be destroyed due to excessive current spike.

Just as for the transconductance, the threshold voltage of the IGBT will decrease with the increase in temperature. Just as variation in transconductance will introduce turn–off current spike, large variation in threshold voltage can cause dynamic current imbalance because one device will turn off faster than the other device. During the static operation, the threshold voltage will have no effect. However, the decrease in transconductance counterbalances the effect of the decrease in threshold voltage, and the current spike is independent of the temperature.

USING COMMON HEATSINK

With common heatsink, the parameter variation in both devices will approximately be equal, and as a result, the dynamic turn–off current imbalance will not be improved significantly if the designer did not pay attention to the V_{th} and Kp. In fact, using a separate heatsink will actually improve the dynamic current sharing for the IGBTs. Static current sharing is greatly improved in IGBTs because the lifetimes of the devices tend to increase proportionally to other devices with temperature. Using a common heatsink will improve the static current sharing, but large dynamic instability can still be introduced if Kp and V_{th} variation is not minimized.

EFFECT OF CIRCUIT LAYOUT

Just as in normal operation of the single device, the circuit layout is very important in the parallel operation of the devices. Large variation in common–emitter inductance has been shown to be the biggest contributor to the cause of dynamic current imbalance of the devices. If one of the device's emitter–ground inductance is large while the other device sees low inductance, a large current spike is observed by the lower inductance device because it turns on much faster than the other. It was discussed earlier that the large emitter inductance introduces large voltage drop and results in clamping of the gate current during the turn–on. So more of the gate current is diverted to the device with lower common–emitter inductance. With the interaction of parasitic capacitors and nonlinear voltage–dependent junction capacitance of the devices, it will oscillate with large common–emitter inductance. This will be sensed by the other device, and they will together oscillate out of phase with each other.

EFFECT OF GATE RESISTANCE

If separate gate resistors are used for each device, it will introduce a variation in delay time (or storage time). The device with longer turn–off time will stay on longer, and the lower storage time device will transfer its current to the other

device. This will introduce more power dissipation in one device and introduce thermal instability if separate heat sinks are used.

If careful attention has been given to the circuit layout, and common–emitter inductance has been minimized, using a single–gate resistor for both devices will reduce the turn–off storage time variation because the device with higher storage time will keep the other device conducting to a value which is dependent on the device transconductance.

SUMMARY

Many of the problems associated with paralleling of power devices can be greatly reduced by using IGBTs. It has been shown that the device characteristics of the IGBT device favors parallel operation as opposed to BJTs. Its dual device characteristics can be utilized to give design engineers very satisfactory performance under static and dynamic current sharing of the devices. Problems associated with paralleling IGBTs can be minimized and deterred if careful attention is given to parameter variations, careful circuit layout (minimizing parasitic inductance), and using common heatsinks. Remember that using a common heatsink does not improve the dynamic current imbalance if parameter variations of Kp and V_{th} are large. Static current sharing is increased with the use of common heatsink. Most of the failure of the devices in paralleled operation can be contributed to neglect of device temperature effect and not derating the parts as they should have.

In summary, the following criteria should be met for paralleling IGBTs:

1. Minimize the spread of lifetime, Kp, and V_{th} between the devices to be paralleled
2. Minimize the common–emitter inductance difference
3. Take all the precautions just as if the devices were operating as single devices
4. Use single gate resistors to drive the gates to reduce the storage time variations
5. Use a common heatsink for all of the devices
6. Understand which characteristics will dominate the parallel operation (BJT or MOSFET)
7. Calculate the junction temperature using worst case numbers

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