Research Report

Investigation of Short-circuit Capability of IGBT under High Applied Voltage Conditions

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Abstract

We have investigated a new short-circuit failure mode of an Insulated Gate Bipolar Transistor (IGBT) occurring under high applied voltage, by experiments and device simulation. The failure mode is characterized by abrupt destruction within a few microseconds after turning on the transistor. This phenomenon is caused by concentration of the hole-current generated by dynamic avalanche at an emitter contact edge of the active cells. In addition, the hole-current path was changed by the gate voltage. This hole-current concentration caused sudden degradation of the short-circuit capability when the gate voltage exceeded a certain value. By preventing the hole-current concentration, we developed an IGBT with sufficient short-circuit capability of more than 10μsec under a high applied voltage.

Keywords: Dynamic avalanche, Short-circuit capability, Turn-on failure, High applied voltage, IGBT (Insulated Gate Bipolar Transistor)

1. Introduction

Insulated gate bipolar transistors (IGBTs) have been used as switching devices for inverters. Increasing the voltage applied to an inverter is an effective way for increasing the motor output power. However, a higher applied voltage tends to lower the short-circuit withstand capability of the device, because energy dissipation during the turn-on period increases with the applied voltage. It is therefore important to design the device so as to withstand short-circuit condition under a high applied voltage.

Many studies on IGBT short-circuit robustness have been reported. In earlier studies, four types of short-circuit failure modes were reported.[1-7] The short-circuit failure modes are schematically shown in **Fig. 1**. Mode [A] is destruction occurring during the few microseconds after turn-on, due to the latch-up of the device when a huge collector current is applied. Mode [B] is thermal destruction caused by excessive power dissipation during the turn-on period. Mode [C] is destruction observed during turn-off period. Mode [D] is destruction observed a few hundred microseconds after turning off the gate. This mode is described as thermal runaway caused by leakage current.

We observed a new failure mode characterized by abrupt lowering of short-circuit capability when both the applied voltage and the gate voltage exceed a certain value, as shown in **Fig. 2**. The short-circuit capability is decreased when a higher voltage is applied under short-circuit conditions, because the power dissipation increases. Specifically, the capability is suddenly decreased when the gate voltage exceeds about 15V. As far as we know, this mode is different from any other mode reported up to now.

In this paper, we investigated this new turn-on failure mode. We also developed a very rugged IGBT with a rating current of 200A, achieved through a structure preventing this new turn-on failure mode.

2. New turn-on failure mode

In this section, the new turn-on failure mode is discussed on the basis of experimental results.

2. 1 Short-circuit waveform

Although this turn-on failure occurs under high applied voltage, the peak current at that time was found to be much less than that of a low applied voltage where the short-circuit current is successfully turned off, as shown in **Fig. 3**. The value of the peak current does not seem to be directly related to the destruction. Many researchers have reported that the mode [A] can be explained as a latch-up caused by parasitic bipolar action.[1-7] Here, the magnitude of the conduction current is probably a key factor for triggering the destruction mode. However, the destruction mode indicated in Fig. 3 is clearly different from the mode [A].

2. 2 SEM image of the destruction trace

The visible results of the local destruction were

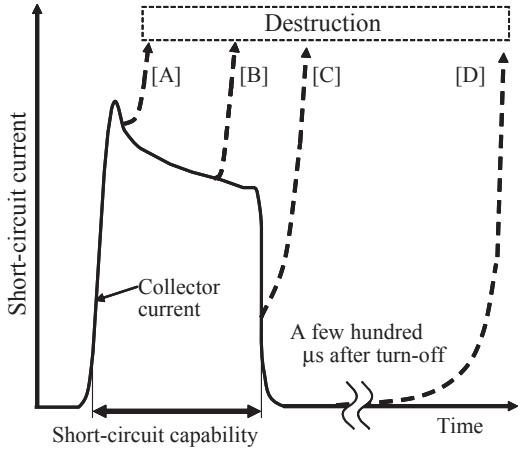

Fig. 1 Schematic view of short-circuit failure modes.

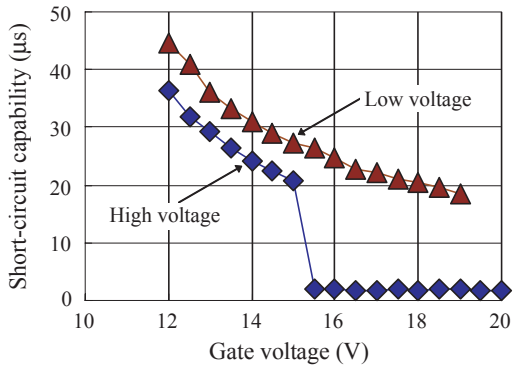

Fig. 2 Dependence of short-circuit capability on gate voltage in the cases of low and high applied voltage.

observed with a scanning electron microscope (SEM), as shown in **Fig. 4**. The destruction point was always located at the emitter contact edge of the active area close to the device's peripheral region, and the impurity profile at that point was high-doped of p^+ region. This implies that huge hole-current concentrated at this point within a short period of time after turning on the device. This destruction mechanism is different from latch-up.

3. Device simulation analysis

In this section, the device simulation was carried out using a model structure of the area of destruction to clarify the abrupt turn-on failure mechanism.

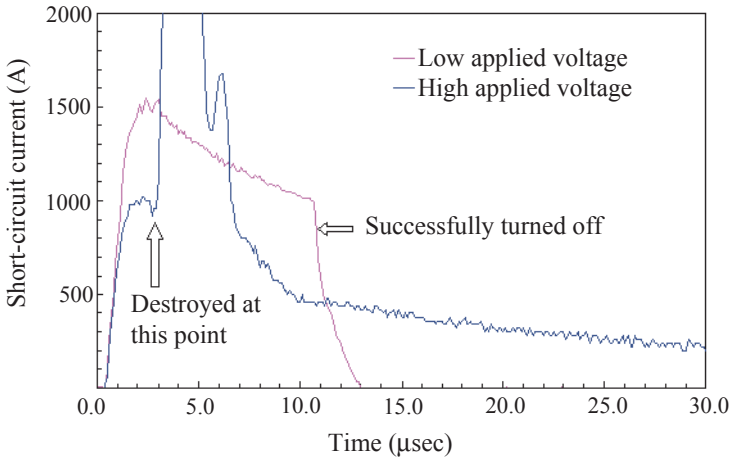

Fig. 3 Short-circuit current waveforms in the cases of low and high applied voltage.

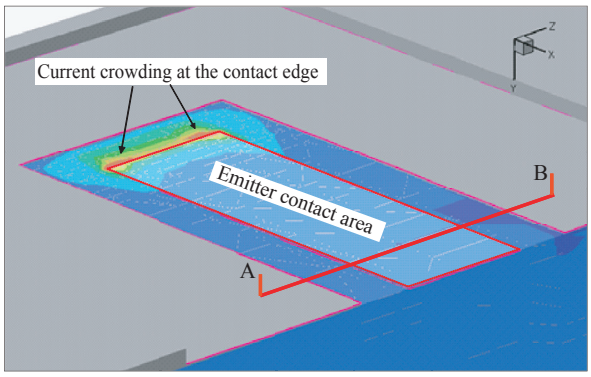

Fig. 5 3D-simulation result of hole-current density distribution in on-state.

3. 1 Current crowding at emitter contact edge

Figure 5 shows a three-dimensional simulation result of the hole-current density under high applied voltage. It is clear that the hole-current concentrates at the edge of the electrode contact with the emitter, and that the current concentration point matches the destruction point observed in Fig. 4.

3. 2 Abrupt destruction mechanism during the turn-on period

Figure 6 shows a cross-sectional view of the A-B portion in Fig. 5. Point A corresponds to the deep p^+ region of the device peripheral region. The destruction time of the measured samples showed excellent correlation with the time of maximum hole avalanche generation rate at point A as shown in **Fig. 7**. This hole current caused by the avalanche generation flow to the emitter contact. However, the resistance against movement of holes in the A-B direction increases with the gate voltage.

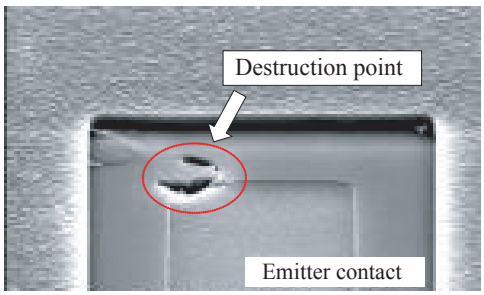

Fig. 4 SEM image of destruction trace caused by new turn-on failure mode.

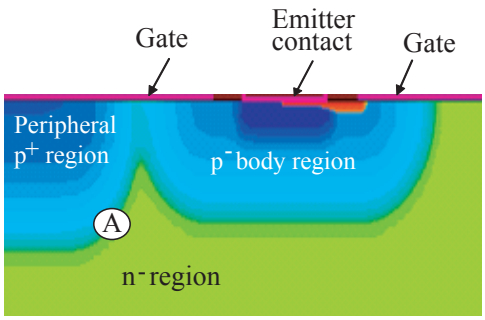

Fig. 6 Cross-sectional view of line A-B in Fig. 5.

The reason is as follows. Firstly, a parasitic PMOS is formed between the p^- body and the peripheral p^+ region. Here, the avalanche hole current under the gate is subjected to the gate potential and is detached from the surface when the gate voltage is increased. Thus the resistance between the p^- body and the p^+ peripheral regions increases with the gate voltage.

If the resistance of the p^+ peripheral region is lower than that of the parasitic PMOS, the hole-current tends to flow in the X direction of Fig. 5 under high gate voltage conditions. As a result, the avalanche current tends to change its flow path with change in the gate voltage. Specifically, the avalanche current concentrates at an emitter contact edge when the gate voltage is high.

To verify the above mechanism, IGBTs with ratings of 200A and 850V were fabricated. On the basis of the model mentioned above, we changed the peripheral structure of the device so as to make the current flow caused by the avalanche generation more uniform. As a result, we confirmed that a short-circuit capability of more than 10μsec was achieved for gate voltages up to 20V even under a high voltage operation of 600V, as shown in **Fig. 8**.

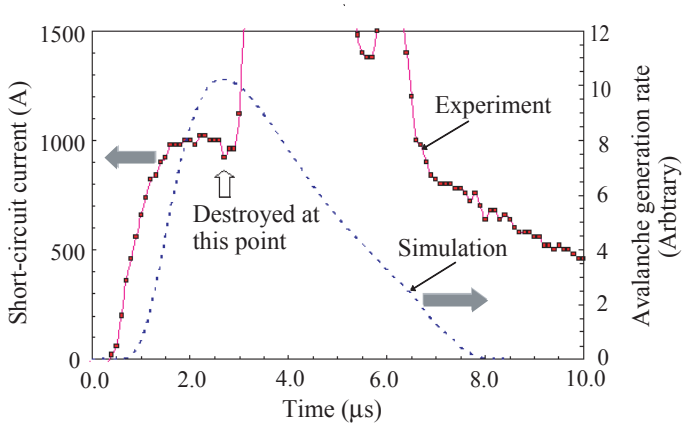

Fig. 7 Current waveform of the new turn-on failure mode and simulated avalanche generation rate of hole carrier at point A in Fig. 6.

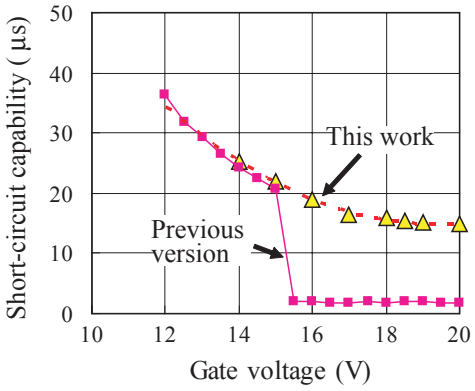

Fig. 8 Improvement of the short-circuit capability under high applied voltage by uniform dynamic avalanche condition.

4. Conclusion

A new IGBT turn-on failure mode has been investigated. The failure mode is characterized by abrupt destruction after a few microseconds under the short-circuit conditions of high collector and gate voltages. This is due to hole-current caused by dynamic avalanche generation during the turn-on period, concentrated at an emitter contact edge. The short-circuit capability under high driving conditions was improved by making the current flow more uniform.

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