Semicond. Sci. Technol. **13** (1998) 806–815. Printed in the UK PII: S0268-1242(98)91088-4

A simulation study of high voltage 4H-SiC IGBTs

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Received 27 January 1998, accepted for publication 7 April 1998

Abstract. This paper evaluates the performance of high voltage 4H-SiC IGBTs. The static and dynamic characteristics of SiC IGBTs with various high voltage ratings and structures at different temperatures are obtained by 2D numerical and analytical simulations. Discrepancies in the device performance are investigated. Comparison with silicon IGBTs is also included.

1. Introduction

Wide bandgap SiC is a desirable material for power devices due to its superior properties such as high critical electric field, high saturation velocity, low leakage current, wide operating temperature range and high thermal conductivity. It is anticipated that the development of SiC devices will enhance current technologies in applications where high power, high speed and high temperature are needed. Among the various SiC polytypes, the higher electron mobility and wider bandgap of 4H-SiC makes it particularly important.

The advent of the insulated-gate bipolar transistor (IGBT) solved the main problem of the silicon metal oxide–semiconductor field-effect transistor (MOSFET): that of rapid degradation of the current handling ability with increased voltage rating. Being minority carrier devices, the current handling ability of IGBTs is not affected by the resistivity of the drift region as severely as with MOSFETs. Sharing many of the appealing features of power MOSFETs, such as ease of drive, wide safe operation area (SOA), peak current capability and ruggedness, silicon IGBTs have displaced silicon bipolar junction transistors (BJTs) in medium and high voltage applications.

However, their current handling ability cannot compete with silicon thyristors and gate turn-off thyristors (GTOs). Meanwhile, the silicon light-triggered thyristor is the only device available meeting the power rating requirement of modern high voltage direct current (HVDC) transmission systems. The phase-controlled three-phase full-bridge converter used in HVDC has many disadvantages such as low power factor under deep control and high harmonic components. Nevertheless, to turn off the thyristor, the voltage across the device must reverse, thereby limiting the kinds of converter configuration that can be used. If high voltage SiC IGBTs are commercially available in the future, the conventional phase-controlled three-phase full-bridge converters used in HVDC systems can be replaced by other kinds of converter with better performance, in which punch-through (PT) IGBTs can be employed to minimize device power losses.

SiC bipolar devices exhibit a relative high built-in voltage (2.7 V) compared to their silicon counterparts (0.7 V); hence, the on-state voltage drop is at least 2.7 V, mitigating the conductivity modulation property of bipolar devices. In addition SiC unipolar devices show much lower specific on resistances than their silicon counterparts. As a consequence SiC IGBTs with low and medium voltage rating are not projected to compete with SiC MOSFETs. This is the same as with the corresponding silicon devices.

For the reasons stated above, this paper aims to investigate the performance of high voltage 4H-SiC IGBTs by employing a 2D physically based numerical simulation package [1] and a 2D on-state analytical IGBT model [2] respectively. The voltage rating is varied from 6 kV to 10 kV and different IGBT structures are studied.

The numerical simulator solves coupled, non-linear partial differential semiconductor physics equations and predicts the electrical characteristics that are associated with specified physical structures and bias conditions.

2. Physical models

In order to achieve realistic results, it is imperative to use accurate SiC property models. The most important physical models employed in the numerical simulations are described as follows.

2.1. Low-electric-field mobility

The low-electric-field mobility is modelled by the Caughey–Thomas equation [3]:

$$\mu_n = \frac{947(T/300)^{-2}}{1+[(N_D+N_A)/1.94\times 10^{17}]^{0.61}} \quad (\mathrm{cm^2\ V^{-1}\ s^{-1}}) \tag{1}$$

$$\mu_p = 15.9 + \frac{124(T/300)^{-2.5}}{1+[(N_D+N_A)/1.76\times 10^{19}]^{0.34}} \quad (\mathrm{cm^2\ V^{-1}\ s^{-1}}) \tag{2}$$

where μ_n, μ_p are the mobility of electrons and holes respectively, N_D, N_A are ionized impurity concentrations.

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2.2. Inversion layer mobility

Due to the lack of inversion layer mobility experimental data for SiC, the Shirahata inversion layer mobility model [1] is used. It takes into account screening effects in the inversion layer. In the simulations for the p base region of IGBTs, it has an improved perpendicular field dependence for thin gate oxides.

$$\mu_{n,p,shi} = \frac{\mu_{n0,p0}}{(1+|E_\perp|/E_1)^{p_1} + (1+|E_\perp|/E_2)^{p_2}} \quad (\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}) \tag{3}$$

where $\mu_{n0,p0}$, E_1, E_2, p_1, p_2 are definable parameters and $E_\perp$ is the normal electric field. The parameters are tuned to obtain an average inversion layer electron mobility of 100 $\mathrm{cm}^2\ \mathrm{V}^{-1}\ \mathrm{s}^{-1}$.

2.3. Generation and recombination

The Shockley–Read–Hall (SRH) recombination–generation rate R_{SRH} and Auger recombination rate R_{Au} are as for Si since no data exist for 4H-SiC. The lifetimes of electrons and holes τ_n, τ_p, are modelled as doping level and temperature dependent:

$$\tau_{n,p} = \frac{\tau_{n0,p0}(T/300)^{2.3}}{1+[(N_D+N_A)/N_{n,p}^{SRH}]} \quad \text{(s)}. \tag{4}$$

In the simulations, $\tau_n = \tau_p$ is assumed.

The generation rate of electron–hole pairs due to impact ionization is modelled according to Selberherr [6]. The Selberherr model uses the following expression to describe the field dependence of the ionization rate:

$$\alpha_{n,p} = a_{n,p} \exp\left(-\frac{b_{n,p}}{|E|}\right). \tag{5}$$

Since no measurements of the avalanche ionization rates have been reported for 4H-SiC, the impact ionization parameters for 6H-SiC were used [4]. The temperature dependence of α_n, α_p is as for Si [1].

3. Results and discussion

3.1. Threshold voltage

Figure 1 shows the typical structure of an IGBT. In IGBTs, an inversion layer will form in the p base region under the gate oxide after the gate–emitter voltage V_{ge} exceeds the threshold voltage V_{th}. Electrons flow from the n^+ emitter region to the n base region through this channel, providing the base current for the integral p–n–p^+ transistor. The threshold voltage V_{th} for a MOS system using an n^+ polysilicon gate is given by:

$$V_{th} = \frac{t_{ox}}{\varepsilon_{ox}}(4qN_A\varepsilon_s V_{fp})^{1/2} + V_{ms} + 2V_{fp} \tag{6}$$

where N_A is the doping level of the p base, ε_s, ε_{ox} the permittivity of the semiconductor and silicon dioxide respectively, V_{fp} the difference between the Fermi level and the intrinsic Fermi level, t_{ox} the thickness of the silicon dioxide and V_{ms} the metal–semiconductor function difference.

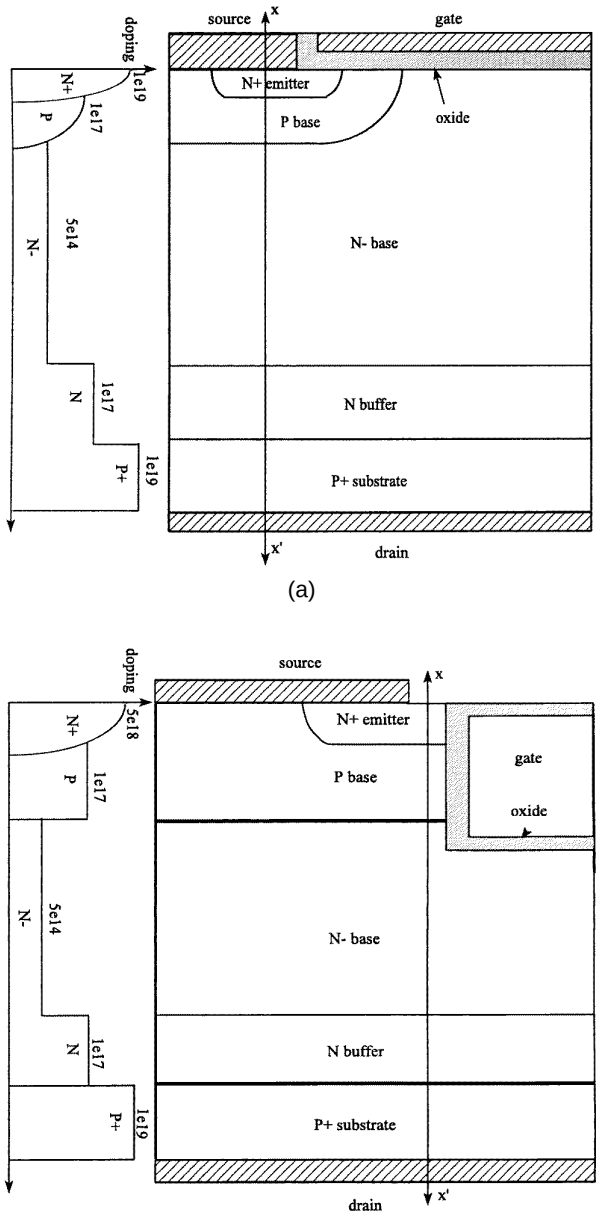


Figure 1. (a) A typical DMOS IGBT cell structure and typical doping profile. (b) A typical UMOS IGBT cell structure and typical doping profile.

Figure 2 shows SiC IGBT threshold voltage against p base doping level at 300 K with an oxide thickness of 500 Å. Silicon IGBT threshold voltages are also shown for comparison. It can be seen that the threshold voltages of SiC IGBTs are higher than the corresponding silicon devices. This is mainly caused by the higher V_{fp} for SiC, which is given by:

$$V_{fp} = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right). \tag{7}$$

Due to the wide bandgap of SiC, its intrinsic carrier concentration is extremely low, only 2.2×10^{-9} cm^{-3} at

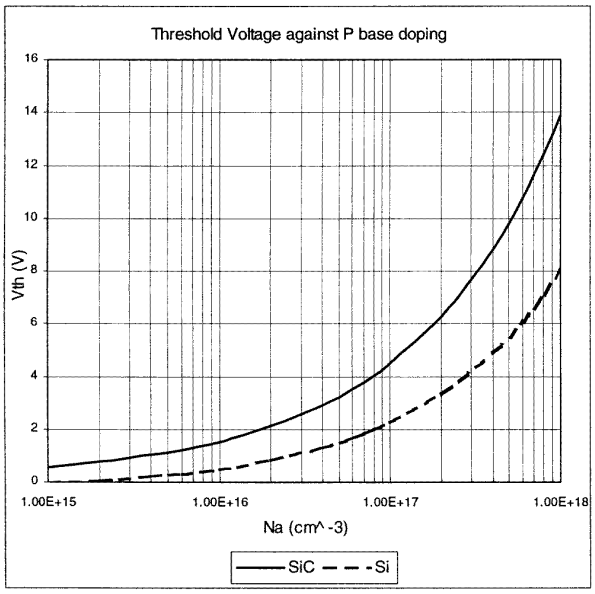


Figure 2. SiC IGBTs threshold voltage against p base doping at 300 K.

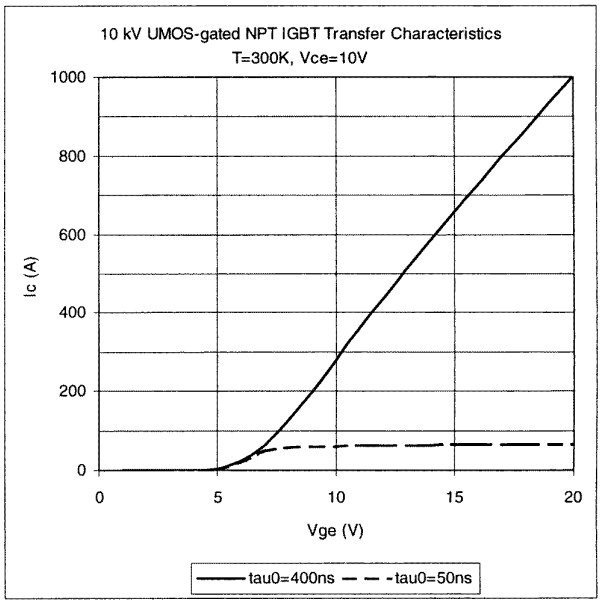


Figure 3. 10 kV UMOS-gated NPT IGBT transfer characteristics.

300 K. In contrast, the intrinsic carrier concentration for silicon is 1.5×10^{10} cm^{-3} at 300 K.

The p base doping level is a critical design parameter affecting V_{th}. For SiC devices, the n base doping level chosen to support the desired blocking voltage is about 100 times higher than that for the corresponding silicon devices. The n base doping level of 10 kV SiC devices is of the order of 1×10^{14} cm^{-3}. Hence to guarantee the depletion layer extends mainly into the n base and to avoid punchthrough of the n$^+$ emitter, the p base doping should be at least 1×10^{16} cm^{-3} for 10 kV SiC devices. Furthermore, the hole current flow must traverse a path beneath the n$^+$ emitter region to reach the emitter electrode. The lateral

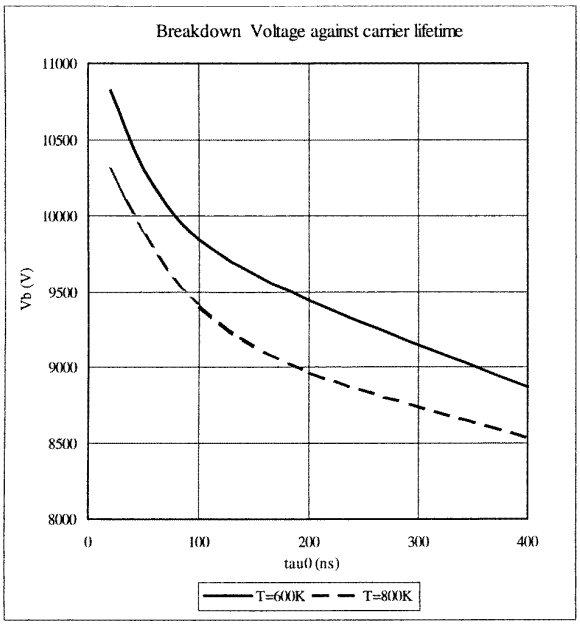


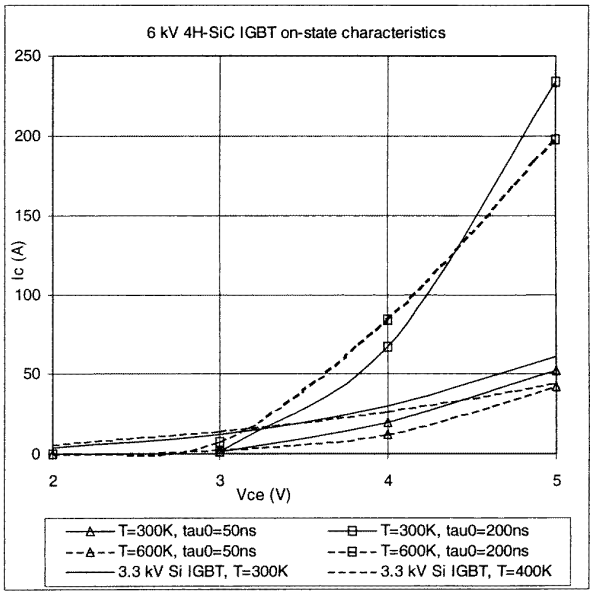
Figure 4. SiC IGBT breakdown voltages against the carrier lifetime.

hole current flow produces a forward bias across the n$^+$–p junction close to the channel [5]. If this voltage bias exceeds the built-in voltage, the parasitic thyristor structure in the IGBT will be activated, thereby losing gate voltage control of the collector current. To prevent latchup, the p base resistance under the n$^+$ emitter must be low, therefore, low p base doping is not suitable. However, high p base doping will result in a high threshold voltage, inducing a high gate drive voltage requirement to maintain the device in its on state. To account for the gate–emitter voltage rise due to parasitic capacitance coupling and to provide enough immunity to external disturbance, a threshold voltage of between 4 and 6 V is suitable. This corresponds to a base doping level of 1 to 3×10^{17} cm^{-3}.

The transfer characteristics of a 10 kV trench IGBT (UMOS IGBT) obtained via numerical simulation are plotted in figure 3. The oxide thickness, the p base doping level and the device area are 500 Å, 1×10^{17} cm^{-3} and 1 cm^2, respectively. The collector–emitter voltage bias is 10 V and the temperature is 300 K. The transfer characteristic for $\tau_0 = 50$ ns shows a transconductance g_m close to zero while the applied gate voltage is greater than 10 V. This indicates that the channel resistance is negligible compared with the n base series resistance in the high gate voltage range. Increasing the carrier lifetime to 400 ns, the collector current rises rapidly with increased gate bias even after entering the high gate voltage bias region. Elevating carrier lifetime reduces the n base series resistance to a value comparable to the channel resistance, hence the n base resistance is no longer a current limiting factor.

3.2. Voltage blocking capability

Non-punch-through (NPT) IGBTs (no n buffer) have symmetrical forward and reverse blocking ability and can be used in AC circuits. In DC circuit applications, only



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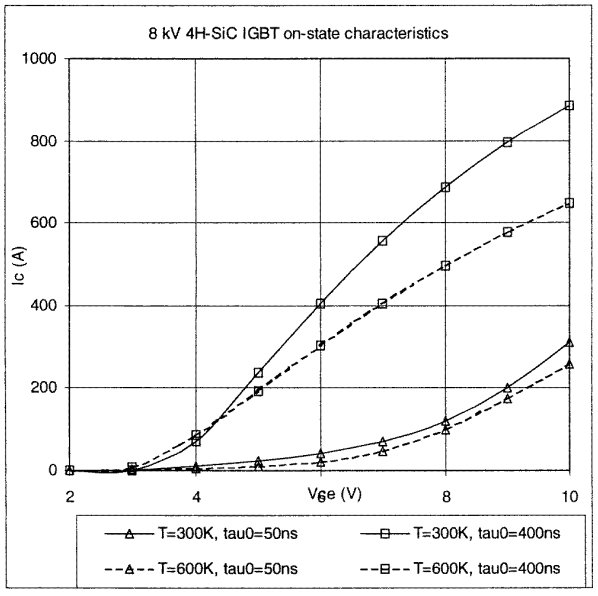
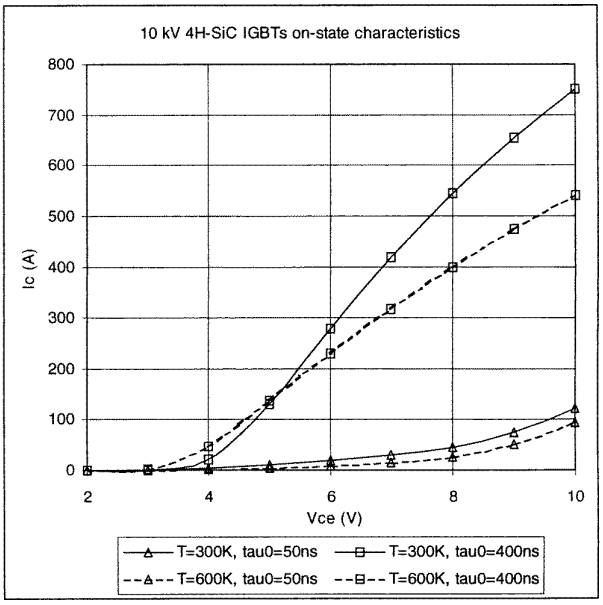


(b)

Figure 5. (a) 6 kV 4H-SiC UMOS PT IGBT on-state characteristics. (b) 8 kV 4H-SiC UMOS PT IGBT on-state characteristics. (c) 10 kV 4H-SiC UMOS PT IGBT on-state characteristics.



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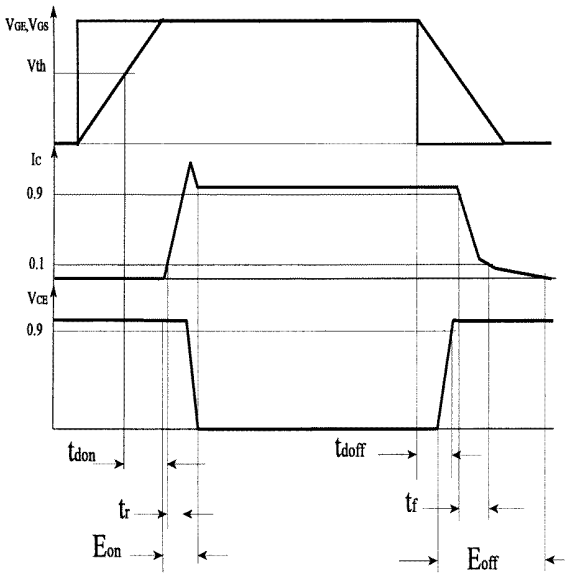


Figure 6. Definition of switching time.

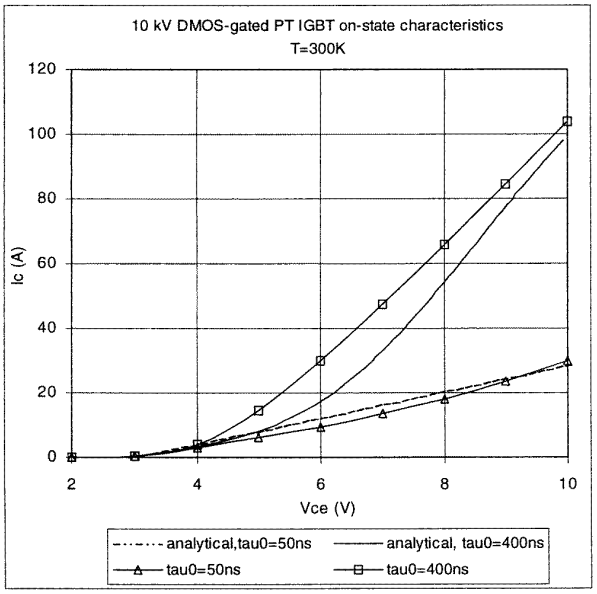
forward blocking is usually required. This affords the use of the punch-through structure to optimize the forward conduction characteristics for a given forward blocking capability, without considering the reverse blocking capability. The forward blocking capability of IGBTs is determined by the open-base breakdown voltage of the integral p base/n base/p^+ collector BJT transistor, which is strongly influenced by minority carrier lifetime in the n base. Open-base pnp transistor breakdown occurs when the product of the multiplication factor M and the current gain α equals unity.

Due to its large n base width which is required for a high blocking voltage, the current gain of the pnp transistor can be approximated by the base transport factor.

$$\alpha_T = \frac{1}{\cosh(W_L/L_a)} \tag{8}$$

where W_L is the undepleted n base width and L_a is the ambipolar diffusion length in the n base determined by the n base high level injection carrier lifetime τ_a and ambipolar diffusion coefficient D_a: $L_a = (D_a\tau_a)^{1/2}$.

A device with longer n base carrier lifetime has a larger L_a, hence a higher current gain. Thus the forward



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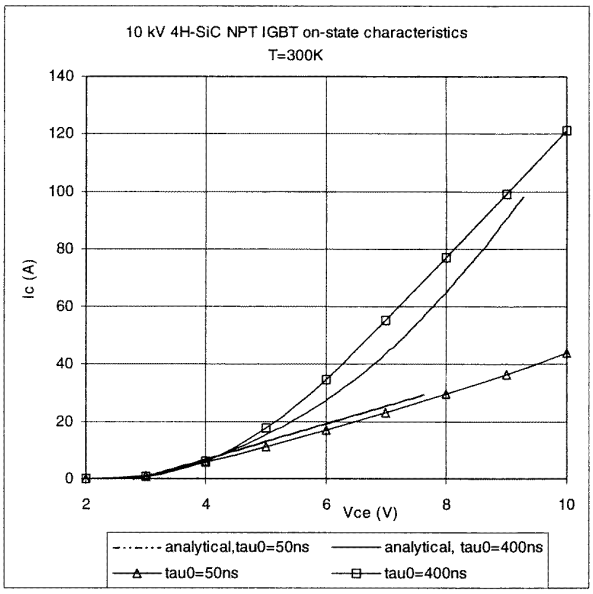

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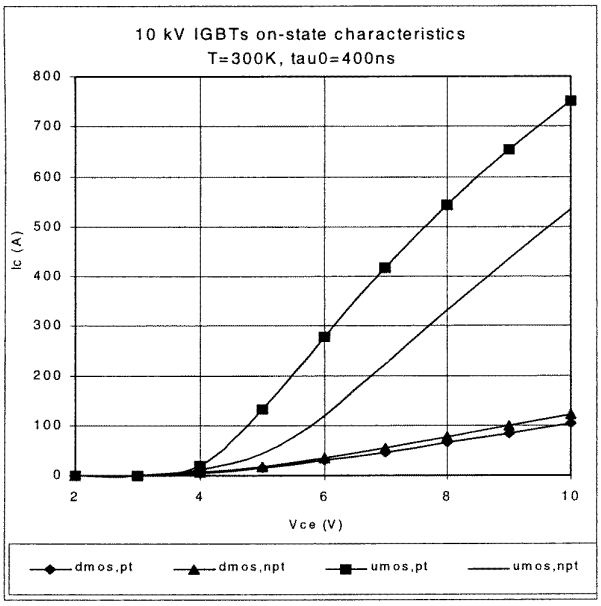
Figure 7. (a) 10 kV 4H-SiC DMOS PT IGBT on-state characteristics obtained using a 2D analytical model. (b) 10 kV 4H-SiC DMOS NPT IGBT on-state characteristics obtained using a 2D analytical model.



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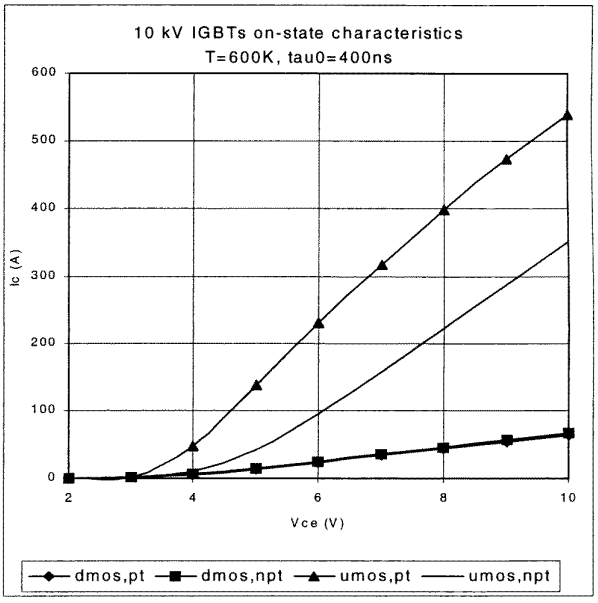
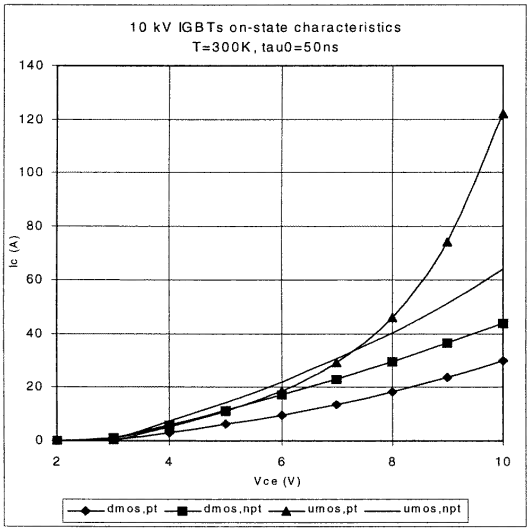


(b)

Figure 8. (a) 10 kV 4H-SiC IGBTs on-state characteristics, T = 300 K, τ_0 = 400 ns. (b) 10 kV 4H-SiC IGBTs on-state characteristics, T = 600 K, τ_0 = 400 ns. (c) 10 kV 4H-SiC IGBTs on-state characteristics, T = 300 K, τ_0 = 50 ns. (d) 10 kV 4H-SiC IGBTs on-state characteristics, T = 600 K, τ_0 = 50 ns.

blocking voltages of IGBTs degrade with increased carrier lifetime. Figure 4 shows the reduction of the forward blocking capability of SiC IGBTs with increased lifetime. A device with a carrier lifetime of 400 ns has a forward breakdown voltage 2 kV less than a device with a 20 ns carrier lifetime.

For SiC IGBTs designed for high temperature operation, the impact of temperature on the breakdown voltage must be taken into account. The multiplication factor M decreases with temperature, because the impact ionization coefficients decrease with temperature due to enhanced scattering of free carriers at elevated temperature. In contrast, carrier lifetime increases with temperature, producing a rapid increase in current gain. However, carrier mobility also decreases with temperature, mitigating the impact of lifetime on current gain to some extent. Figure 4 shows the forward blocking voltages of a 4H-SiC UMOS PT IGBT at 600 K and 800 K. The breakdown voltages at 600 K are 300–500 V higher than those at 800 K. When designing the device, the breakdown voltage must be measured at the



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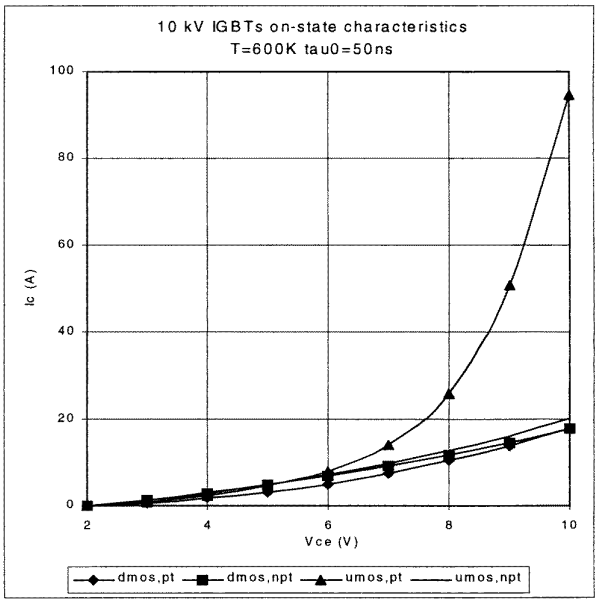

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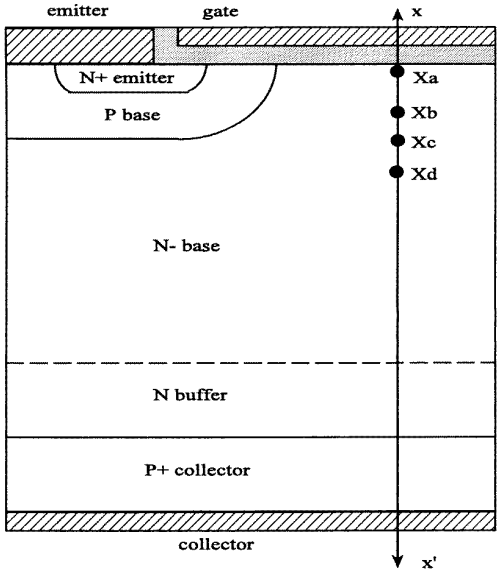
Figure 8. (Continued)



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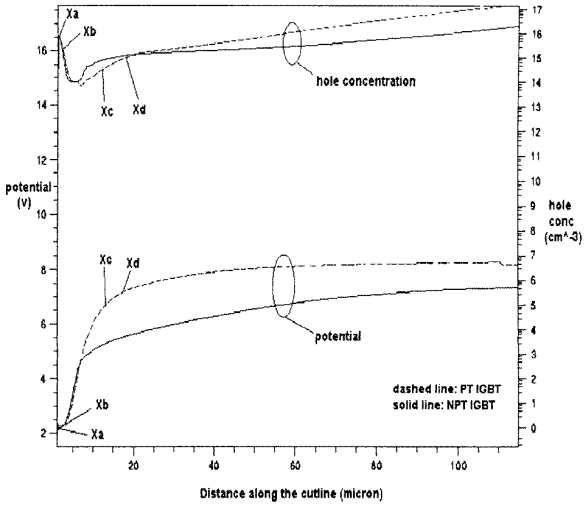


(b)

Figure 9. (a) SiC DMOS IGBT cell structure. (b) On-state electric field and hole concentration distribution in SiC IGBTs.

maximum operating temperature. In this work, SiC lifetime varies with temperature according to $T^{2.3}$ [1].

3.3. On-state characteristics

The on-state characteristics of 6 kV, 8 kV and 10 kV UMOS PT IGBTs with $V_{ge} = 15$ V are simulated and shown in figure 5. The on-state characteristic of a 3.3 kV, 1.2 kA Si IGBT is also included for comparison. The cell pitch is 30 μm and the device area for the SiC devices is 1 cm^2. As shown in figure 5(a), the 6 kV 4H-SiC IGBT exhibits better current handling ability than a 3.3 kV Si IGBT in spite of the fact that the built-in voltage $V_{bi,SiC}$ (2.7 V) for SiC is about 2 V higher than $V_{bi,Si}$ (0.7 V). The temperature dependences of SiC IGBTs' conduction characteristics are minimal, just enough to ensure steady state current sharing of parallel connected devices at high current levels. At high current densities, the devices show a current saturation trend, which is favourable for practical use.

3.4. Switching characteristics

Table 1 shows the simulated switching characteristics for 6 kV, 8 kV and 10 kV UMOS PT IGBTs with a clamped inductive load. The ringing between circuit parasitic inductance and diode capacitances affects simulation convergence and speed. So in this paper parasitic inductance effects are neglected. The performance of the clamping diode, especially diode reverse recovery, effects the turn-on characteristics of the IGBTs. In this paper, the analytical diode model integrated in the simulator is used. The device areas are 1 cm^2. The devices are turned on and

Table 1. High voltage 4H-SiC UMOS IGBT switching characteristics.

Voltage rating	Conditions	T (K)	τ_0 (ns)	$t_{d(on)}$ (ns)	t_r (ns)	$t_{d(off)}$ (ns)	t_f (ns)	E_{on} (mJ)	E_{off} (mJ)
6 kV	J_{on} = 100 A cm^{-2},	300	50	31	12	55	130	28.3	34.6
			200	31	12	140	320	24.4	92.6
	A = 1 cm^2, V_s = 3 kV	600	50	37	15	130	420	28.8	77.4
			200	38	16	150	2130	25.2	413
8 kV	J_{on} = 75 A cm^{-2},	300	50	27	13	140	48	25.5	35
			400	27	13	140	46	19.8	198.3
	A = 1 cm^2, V_s = 4 kV	600	50	26	13	140	460	25.7	94.4
			400	28	14	160	1680	20.6	862
10 kV	J_{on} = 50 A cm^{-2},	300	50	33	7	130	40	8.6	27.4
			400	33	8	140	360	7.4	129.7
	A = 1 cm^2, V_s = 5 kV	600	50	26	10	140	270	17.5	70
			400	33	12	150	1610	14.6	592

off by increasing the gate drive circuit supply from 0 V to 15 V and vice versa. The definition of switching times $t_{d(on)}$, $t_{d(off)}$, t_r and t_f can be extracted from figure 6. As shown in table 1, the switching losses increase rapidly with lifetime and temperature.

3.5. Various structures

IGBTs are classified as double-diffused (DMOS) and UMOS IGBTs according to their gate structures. They can also be classified as PT IGBTs and NPT IGBTs depending on the existence of an n type buffer layer. Hence there are four different IGBT structures: DMOS NPT, DMOS PT, UMOS NPT and UMOS PT IGBTs.

Currently all commercially available high voltage silicon IGBTs are double-diffused DMOS IGBTs. UMOS types are restricted to a few hundred volts. Plotted in the parts of figure 7 are the forward conduction characteristics of 10 kV SiC DMOS IGBTs obtained using a two-dimensional on-state IGBT model and the 2D numerical simulator. The results fit well especially in the low carrier lifetime region.

To compare the current handling capability of different IGBT structures, the on-state characteristics of 10 kV IGBTs are simulated employing the numerical simulator and results are shown in figure 8. For all devices, the cell pitch is 30 μm and the p base doping is 1×10^{17} cm^{-3} to obtain a threshold voltage of around 4 V. Two values of carrier lifetime: 400 ns, 50 ns are chosen to study lifetime impact on device performance. The n base width and doping for the different devices are adjusted to block 10 kV at 800 K. All the devices have an area of 1 cm^2.

UMOS IGBTs exhibit much better current handling ability than DMOS IGBTs. The main factor responsible for this is the JFET component between the p base diffusions in DMOS IGBTs. In addition, the accumulation layer formed under the trench bottom in UMOS IGBTs also improves their on-state characteristics.

Compared with the NPT IGBT, the PT IGBT has an additional n buffer layer to reduce the n base width. In order to support the same breakdown voltages, 50%–75% lower n base doping is required for the PT IGBT than for the NPT IGBT. This difference in n base doping results in only a slight difference in carrier mobilities. The carrier diffusion lengths are nearly the same if the carrier lifetimes are the same in both structures. Hence, the modulated n base region resistivity of the PT IGBT is smaller than that of the NPT IGBT for the former has a thinner n base width. It can be seen in figure 8 that UMOS PT IGBTs exhibit better current handling ability than the corresponding NPT IGBTs in all cases. At 600 K, DMOS PT IGBTs have better forward characteristics than the corresponding NPT IGBTs.

However, at room temperature, DMOS NPT IGBTs show better on-state characteristics than DMOS PT IGBTs. To investigate the reason, two master files are generated in the simulator which contain potential and carrier distribution information for the two structures with a forward current density of 100 A cm^{-2}. Figure 9 shows hole concentration and potential distribution along the cutline X–X′ (figure 1(a)) in the two structures. In both structures, the accumulation layer formed under the gate between the p base diffusions and holes injected from the p base into the n base reduce the n base resistivity from point x_a to point x_b, resulting in a negligible voltage drop. However, between x_b and x_c, the depletion layer which extends into the n base reduces both the carrier concentrations and the width of the current path, leading to a rapid increase of the potential in this JFET region. The resistivity in this region is mainly determined by the n base doping level. Compared to the NPT IGBT, the JFET effect hampers the performance of the PT IGBT more severely because the PT IGBT has a 50%–75% lower doping level than the NPT IGBT. It can be seen in figure 9 that the potential in the PT IGBT increases by 1.5 V more from x_b to x_c than in the NPT IGBT. This is the main reason for the better on-state characteristics of the DMOS NPT IGBT at room temperature. From point x_d, carriers injected from the p^+ collector modulate the resistivity of the n base, hence the potential increases slowly. Because of the smaller base thickness of the PT IGBT, the hole concentration in this device is higher than that of the NPT IGBT.

The hard switching characteristics of the devices with a clamped inductive load have been simulated at temperatures of 300 K and 600 K. The supply voltage is 5 kV and the

Table 2. The switching characteristics of 10 kV IGBTs.

	T (K)	τ_0 (ns)	$t_{d(on)}$ (ns)	t_r (ns)	$t_{d(off)}$ (ns)	t_f (ns)	E_{on} (mJ)	E_{off} (mJ)
UMOS	300	50	33	7	130	40	8.6	27.4
PT		400	33	8	140	360	7.4	129.7
	600	50	26	10	140	270	17.5	70
		400	33	12	150	1610	14.6	592
UMO	300	50	33	7	130	10	11.1	21.4
PT		400	32	14	150	480	22.4	62.3
	600	50	24	5	460	9	9.8	41
		400	37	9	150	1500	21.5	152
DMOS	300	50	27	5	100	38	9.4	13.4
PT		400	30	5	120	360	7.8	104.4
	600	50	23	6	97	230	10	57
		400	26	7	120	1480	9.8	500
DMOS	300	50	28	5	100	2	13.1	12.8
NPT		400	28	5	110	620	11.8	52.8
	600	50	23	6	110	7	13.1	18.7
		400	22	5	110	2120	11.8	152

on-state current density is 50 A cm^{-2}. Table 2 lists the main results. Due to the inaccuracy of the analytical diode model in the simulator, the turn-on losses of the devices with lifetime $\tau_0 = 400$ ns are larger than the turn-on losses of the devices with a 50 ns lifetime.

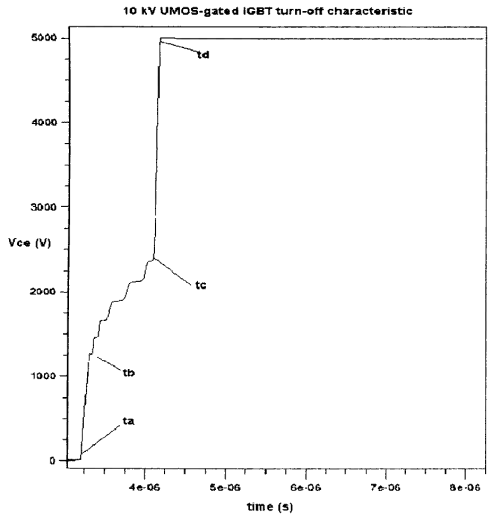
At the same current density, UMOS IGBTs have a lower on-state voltage than the corresponding DMOS IGBTs due to not only the JFET effect but also the larger amount of excess carriers in UMOS IGBTs. As a consequence, UMOS IGBTs have larger turn-off losses than DMOS IGBTs for more excess carriers must be removed.

When comparing the turn-off losses of NPT and PT IGBTs, the PT IGBT structures have larger turn-off losses than the corresponding NPT IGBT structures. A noticeable point of PT IGBT turn-off is a voltage flattening out during the voltage rising phase (figure 10(a)) for the 400 ns lifetime devices, resulting in one to three times higher turn-off power losses than for NPT IGBTs. In figure 10(b)–(c) the hole concentration and the electric field distribution in the base region of the device during turn-off are shown. At room temperature, initially the depletion layer quickly extends into the n base towards the n buffer. At t_b, the voltage waveform flattens out until t_c. It only takes 110 ns ($t_b - t_a$) for the voltage to increase 1200 V. In comparison, it takes 800 ns ($t_c - t_b$) for the voltage to increase another 1200 V. With the aid of figure 10(c), this phenomenon can be explained by the hole concentration distribution in the n base. In the forward conduction state, holes are injected from the p^+ collector into the n buffer and n^- base. The hole concentration in the n^- base has a peak value at the n^- base/n buffer junction, which decays exponentially toward the p base/n base junction. Therefore, a large portion of excess carriers exists in the region near the n^- base/n buffer junction. As indicated in figure 10(c), between t_b and t_c, the stored charges removed from the n base, as a result of the extending depletion layer, are about ten times higher than those between t_a and t_b. At the time t_c, the depletion layer edge reaches the n buffer. Then it extends slightly into the n buffer and the magnitude of the electric field, hence the collector voltage, increases quickly. In NPT IGBT structures, most of the excess carriers in the n base region also exist near the n buffer. However, to support the supplied voltage, the depletion layer edge does not approach the n buffer due to the NPT structure. Therefore, the voltage across the NPT IGBTs increases rapidly and does not slow down as with PT IGBTs. A large amount of excess carriers still remain in the n base at the end of the voltage increase phase. The flattening-out of the voltage in PT IGBTs can be improved by designing the structure carefully so that the n base minority carrier distribution under conduction is more uniform.

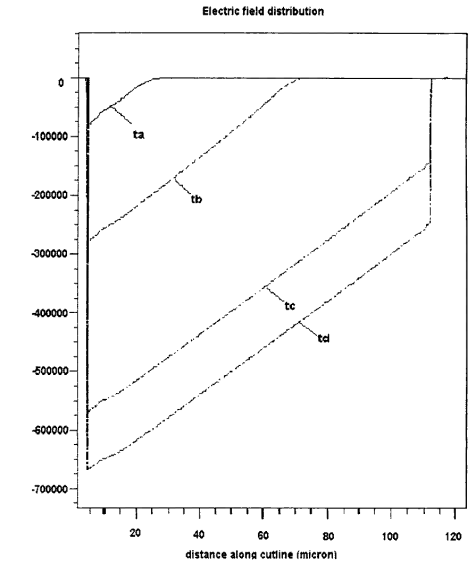
In addition, the power losses of PT IGBTs during the current decrease phase are larger than those of the corresponding NPT IGBTs. As shown in figure 11(a), when the collector voltage exceeds the supplied voltage the diode begins to conduct and the current in the NPT IGBTs drops abruptly to a small value. In contrast, the current in the PT IGBT falls to a higher value and then decays to zero gradually. Although the initial current drop ΔI_c is not equal to $(1 - \alpha_{PNP})I_{on}$, there is a relationship between ΔI_c and the current gain α_{PNP}. The NPT IGBT has a smaller value of α_{PNP} than the PT IGBT, leading to a higher ΔI_c. The remaining stored charge in the NPT IGBT is more than that in the PT IGBT (figure 11(b)). However this charge diminishes by recombination over a long duration, leading to a longer current tail but negligible power losses. The remaining excess carriers in the n buffer of the PT IGBT are removed by the collector current in a short time span.

4. Conclusion

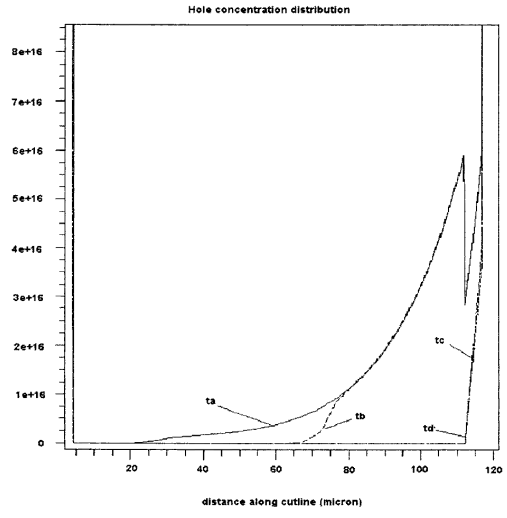
In this paper, the performance of SiC IGBTs with various voltage ratings, lifetime and structure have been simulated using a 2D finite element simulator and a 2D analytical IGBT model. Some characteristics such as threshold voltage versus p base concentration level and breakdown voltage verses lifetime have been simulated and presented.



(a)

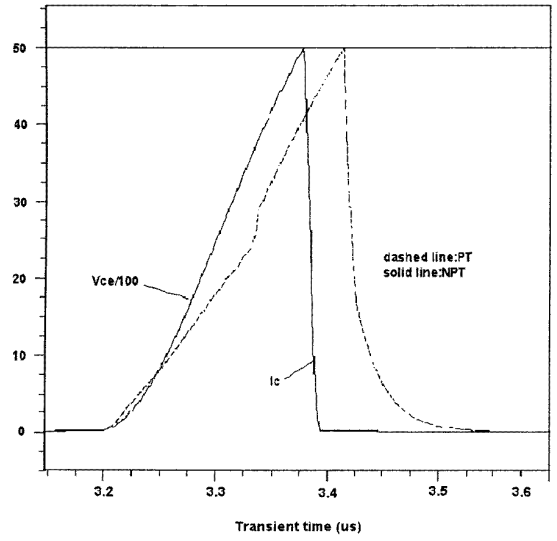


(b)

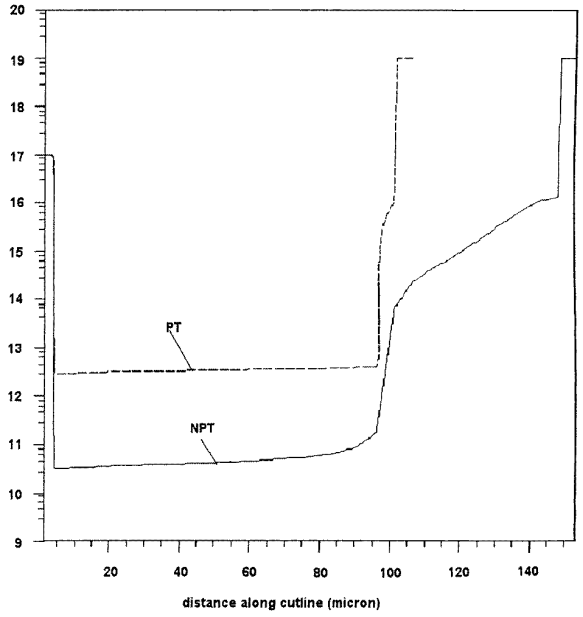


(c)

Figure 10. (a) SiC UMOS PT IGBT turn-off characteristics. (b) Electric field distribution during SiC IGBTs turn-off at T = 300 K. (c) Hole concentration distribution during SiC IGBTs turn-off at T = 300 K.



(a)



(b)

Figure 11. (a) SiC UMOS IGBTs turn-off characteristics. (b) Hole concentration distribution during SiC IGBTs turn-off.

The 6 kV 4H-SiC IGBT shows much better on-state characteristics than a 3.3 kV silicon IGBT. Elevating the temperature to 600 K, the impact of temperature on the current handling ability of SiC IGBTs is minimal. The devices exhibit lower on-state voltages at typical operating currents and a slightly higher on-state voltage at higher current level. This reduces the on-state power losses at typical operating currents and ensures current sharing between parallel connected IGBTs. In contrast, switching losses increase quickly with temperature. The UMOS IGBT has a five to six times better current handling ability than the DMOS IGBT, but its switching power loss is larger due to more excess carriers being stored in the n base region. The PT IGBT has better on-state characteristics than the

corresponding NPT IGBT. However, PT IGBTs exhibit one to three times larger switching power losses, especially with higher lifetimes and at high temperature, partly mitigating the advantage of the PT structure over the NPT structure.

The voltage blocking ability of IGBTs degrades with carrier lifetime increase. For a device with a high lifetime, either its n base doping must be lowered or its n base width must be increased to achieve the required blocking voltage. As shown in section 3.5, a low n base doping induces a large voltage drop across the JFET region of a DMOS IGBT, severely hampering device current handling ability. Taking into account the rapid increase of switching power losses with lifetime and n base width in PT IGBT structures, the carrier lifetime in the DMOS PT IGBT structure should be reduced by lifetime-killing.

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